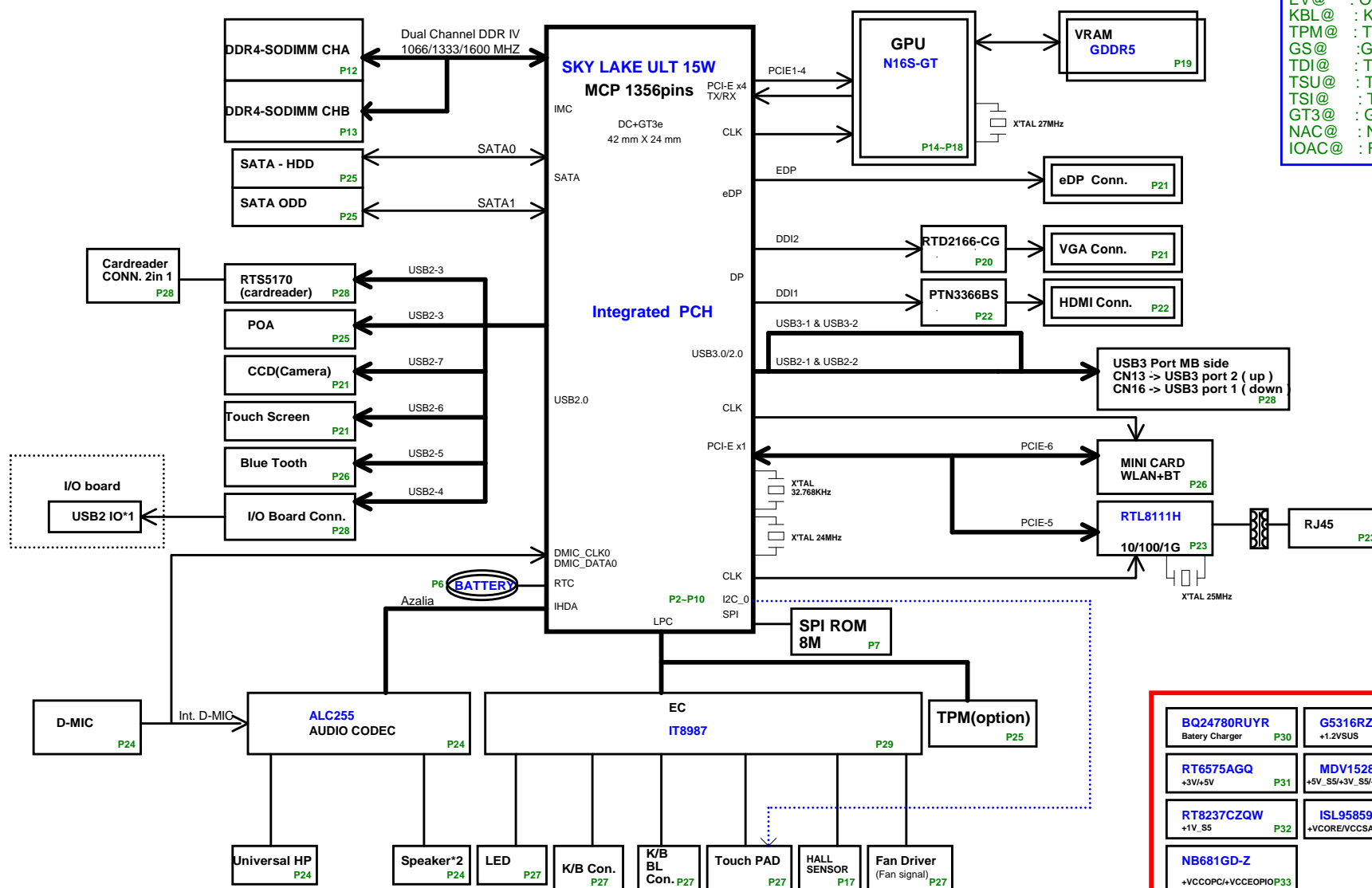


## Z8V Serials SKL ULT SYSTEM BLOCK DIAGRAM

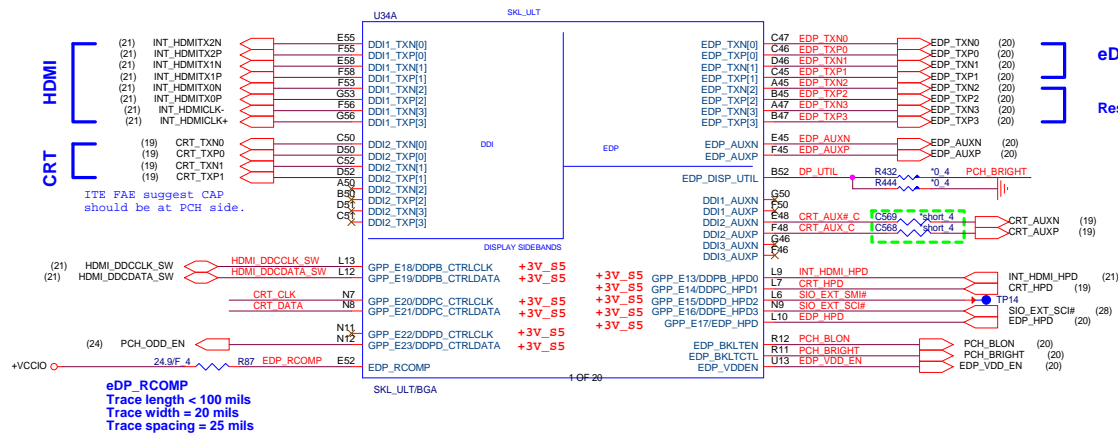


## BOM

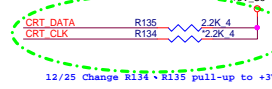
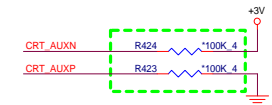
- IV@ : iGPU
- EV@ : Optimus
- KBL@ : Keyboard backlight
- TPM@ : TPM
- GS@ : G-SENSOR
- TDI@ : TOUCH PAD I2C
- TSU@ : TOUCH SCREEN USB
- TSI@ : TOUCH SCREEN I2C
- GT3@ : GT3 CPU
- NAC@ : Non IOAC
- IOAC@ : For IOAC

<b>BQ24780RUYR</b> Battery Charger <b>P30</b>	<b>G5316RZ1D</b> +1.2VSUS <b>P34</b>	<b>Thermal Protection</b> Discharger <b>P38</b>
<b>RT6575AGQ</b> +3V/+5V <b>P31</b>	<b>MDV1528Q</b> +5V_SS/+3V_SS/+3V/+5V <b>P31</b>	<b>UP1658RQKF</b> +VGPU_CORE <b>P39</b>
<b>RT8237CZQW</b> +1V_SS <b>P32</b>	<b>ISL95859HRTZ-T</b> +VCORE/VCCSA/VCCGT <b>P35</b>	<b>RT8068AZQW</b> +1.05V_GFX/+3V_GFX +1.5V_GFX <b>P40</b>
<b>NB681GD-Z</b> +VCCOPC/+VCCOPIO <b>P33</b>		

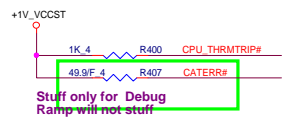
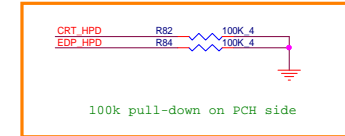
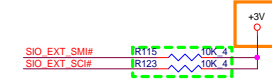
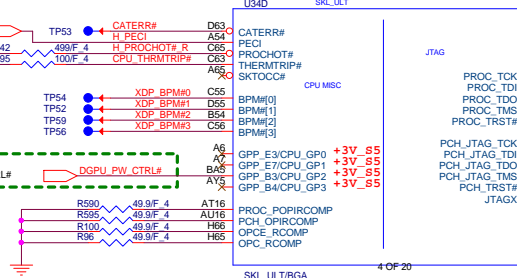
## Skylake ULT (DISPLAY,eDP)



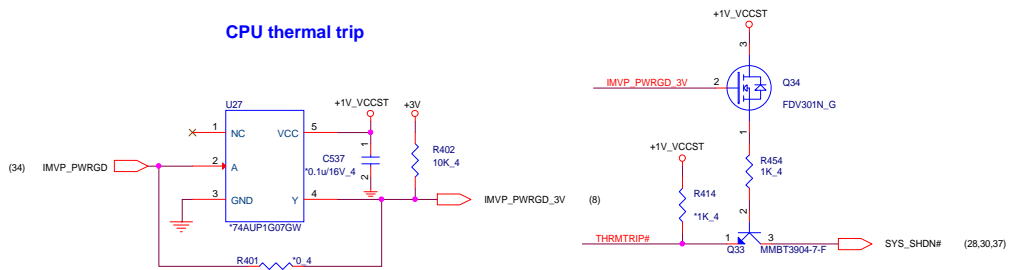
Don't stuff if we use DP to VGA IC



12/25 Change R134, R135 pull-up to +3V\_S5

H\_PECI (50ohm)  
Route on microstrip only  
Spacing > 18 mils  
Trace Length: 0.4-6.125 inchesBPM# [0:7]  
Trace Length 1-6 inches  
Length match < 300 milsSM\_RCOMP [0:2]  
Trace length < 500 mils  
Trace width = 12-15 mils  
Trace spacing = 20 milsIf use Intel DCI USB 3.0 fixtures need to short  
1. XDP\_TDO <-> XDP\_TDO\_CPU  
2. XDP\_TDI <-> XDP\_TDI\_CPU  
3. XDP\_TMS <-> XDP\_TMS\_CPUPCH JTAG  
JTAG\_TCK, JTAG\_TMS  
Trace Length < 9000milsTCK, TMS  
Trace Length < 9000milsH\_PWRGOOD (50ohm)  
Trace Length: 1-11.25 inchesXDP\_TCK1, XDP\_TMS  
don't need pull up or pull down  
XDP\_TCK0 R558 Stuff

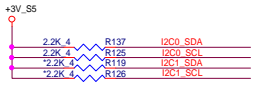
## CPU thermal trip



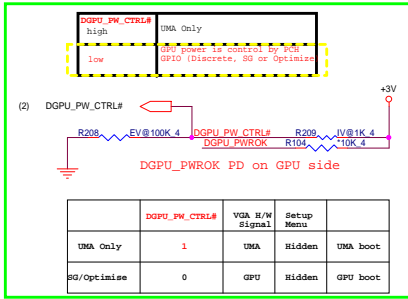
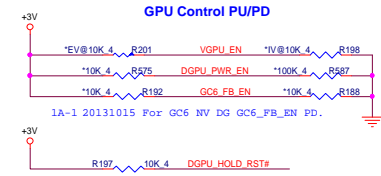


H\_PECI (50ohm)  
If route on microstrip,  
Spacing need >18 mils  
Trace Length: 2-15 inches

H\_PWRGOOD (50ohm)  
Trace Length: 1-11.25 inches



PU 2.2K for touch pad I2C bus (400 KHz)



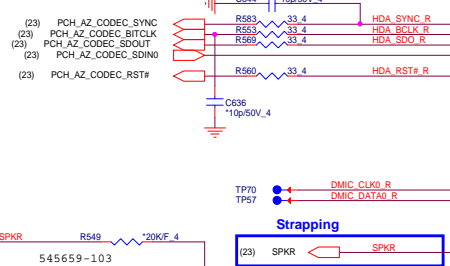
DGPU_PW_CTRL#	VGA H/W Signal	Setup Menu		
UMA Only	1	UMA	Hidden	UMA boot
SG/Optimise	0	GPU	Hidden	GPU boot

UART2 for RMT

Touch PAD

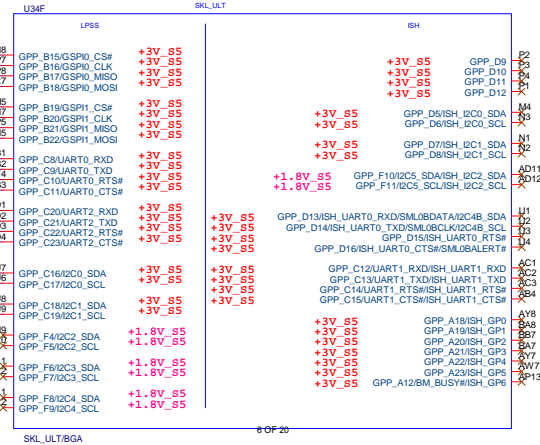
Touch Screen

HDA

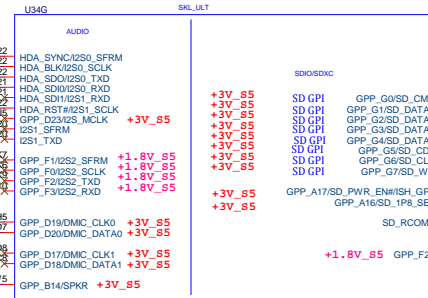


Strapping

545659-103

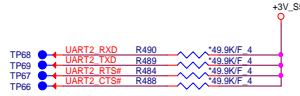


SKL ULT/BGA



SKL ULT/BGA

Reserve UART FFC TP for Win 7 debug

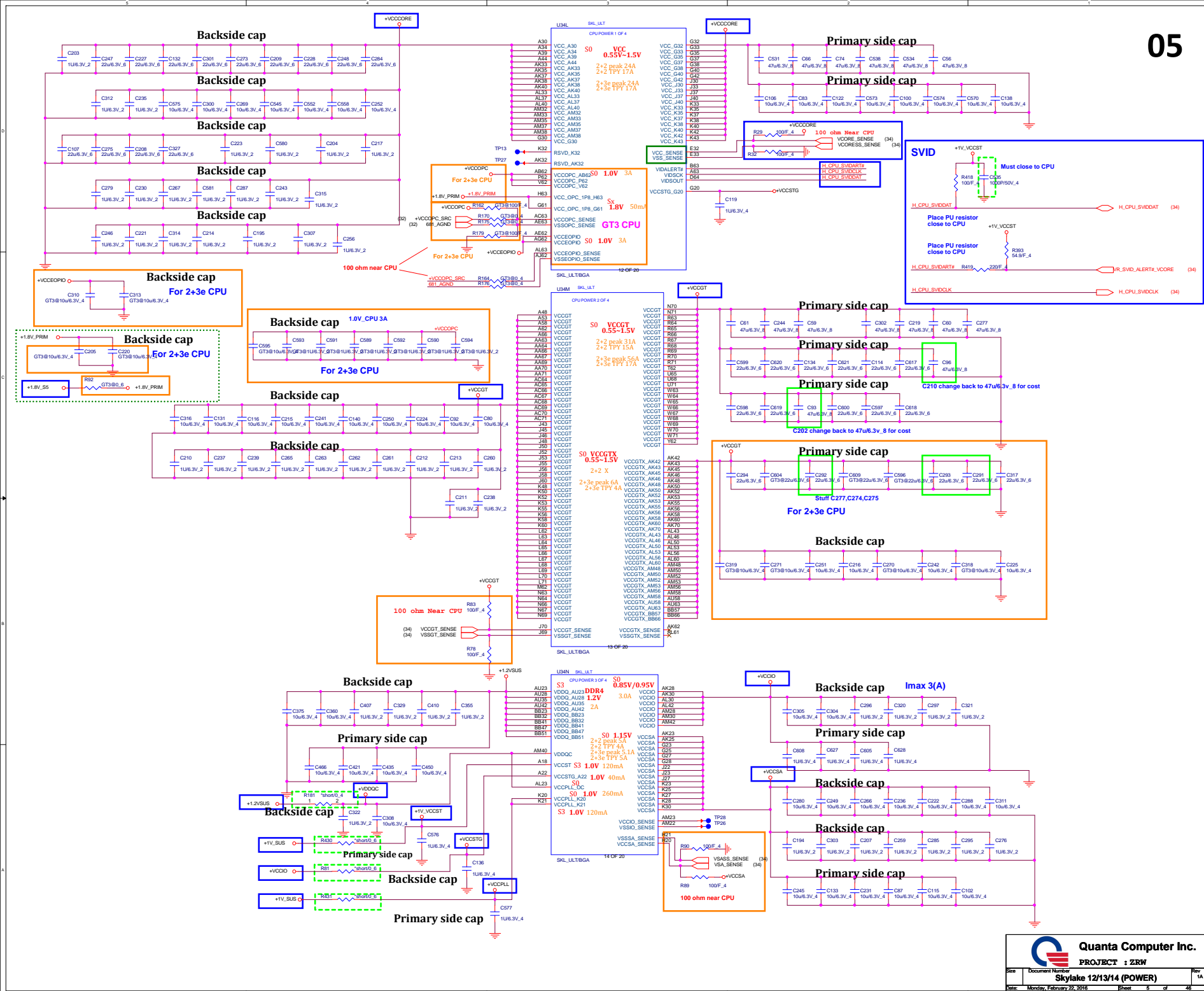


Touchpad INT

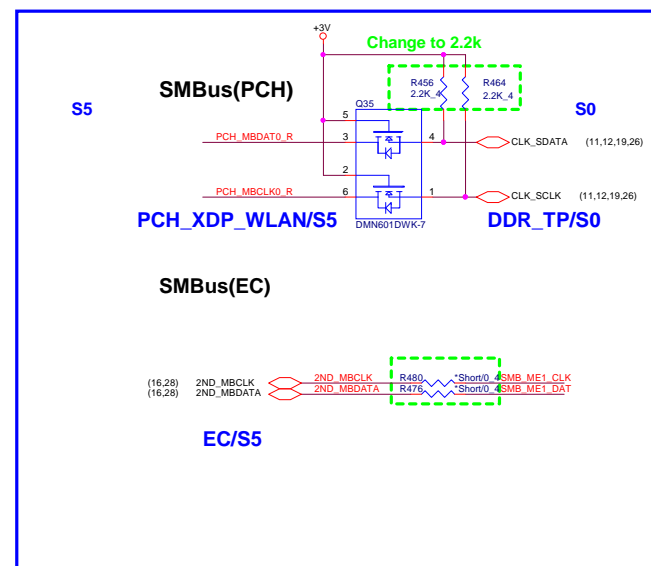


Skylake-U Strapping Table

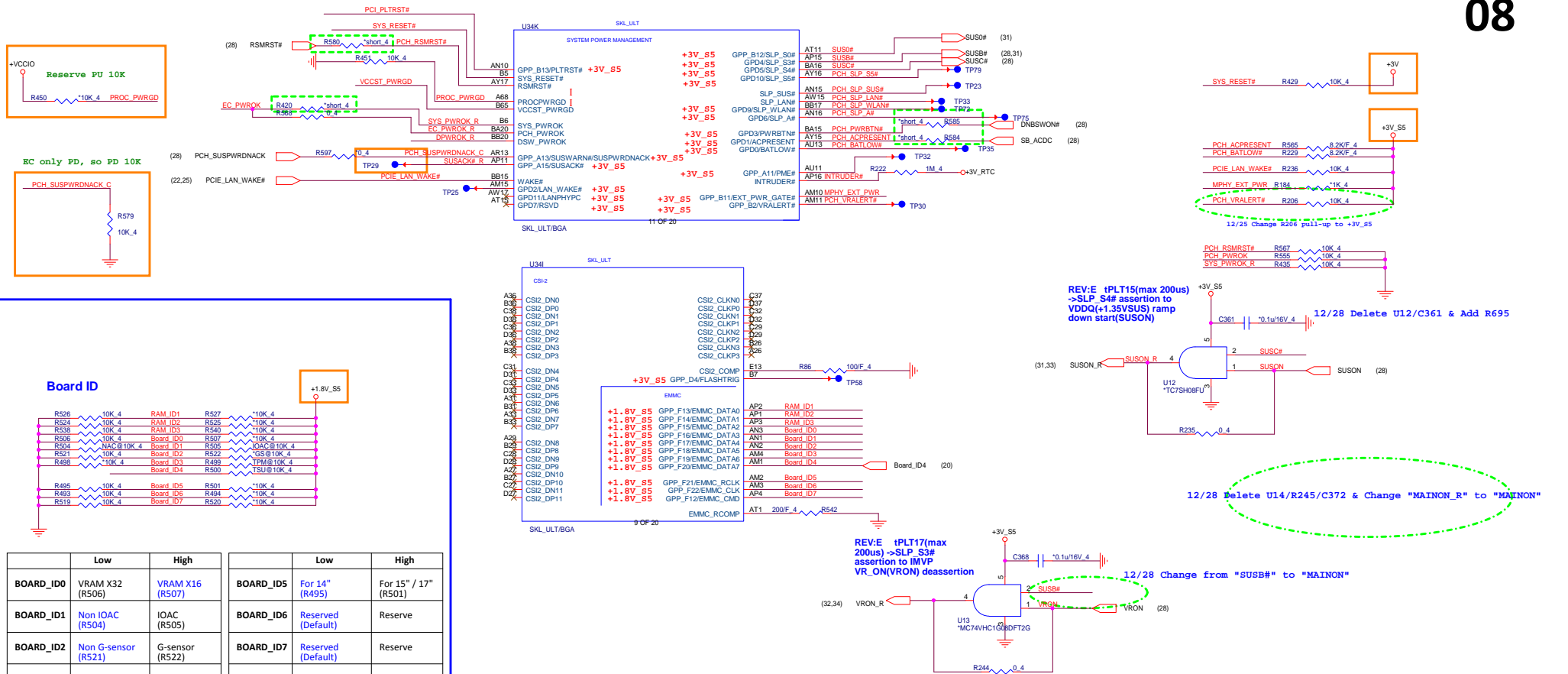
Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (IPD 20K) 1 = Enable Top Swap Mode	3V+ R550 1K 4 SPKR
GPP_B18 (GSP10_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (IPD 20K) 1 = Enable No Reboot Mode	3V+ R543 1K 4 GSP10_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Crypt to TLS (IPD 20K) 1 = Enable Intel ME Crypt to TLS	3V+ SS R144 10K 4 SMBALERT# (7)
GPP_B22 (GSP11_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (IPD 20K) 1 = LPC	3V+ R191 1K 4 GSP11_MOSI
GPP_C5 (SMLOALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (IPD 20K) 1 = eSPI selected for EC	3V+ SS R481 1K 4 SMLOALERT# (7)
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 - 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 - 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 - 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 - 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (IPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal HDA_SDO_R R570 1K 4 ME_WR# (28)
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (IPD 20K) 1 = Port B is detected	
GPP_F21 (DDPB_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (IPD 20K) 1 = Port C is detected	



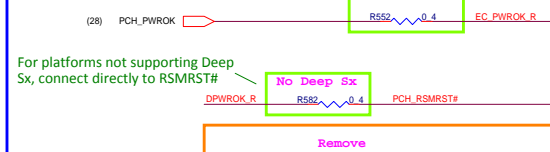




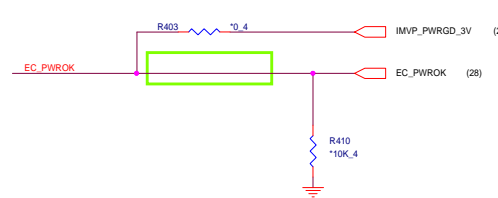
SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR



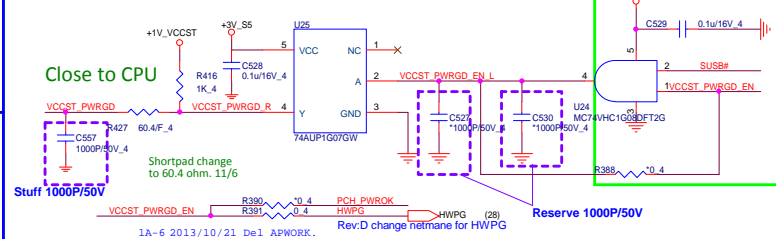
## Power Sequence



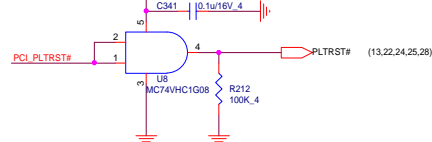
## SYSPWOK



## VCCST PWRGD CRB is via +1.05V PG

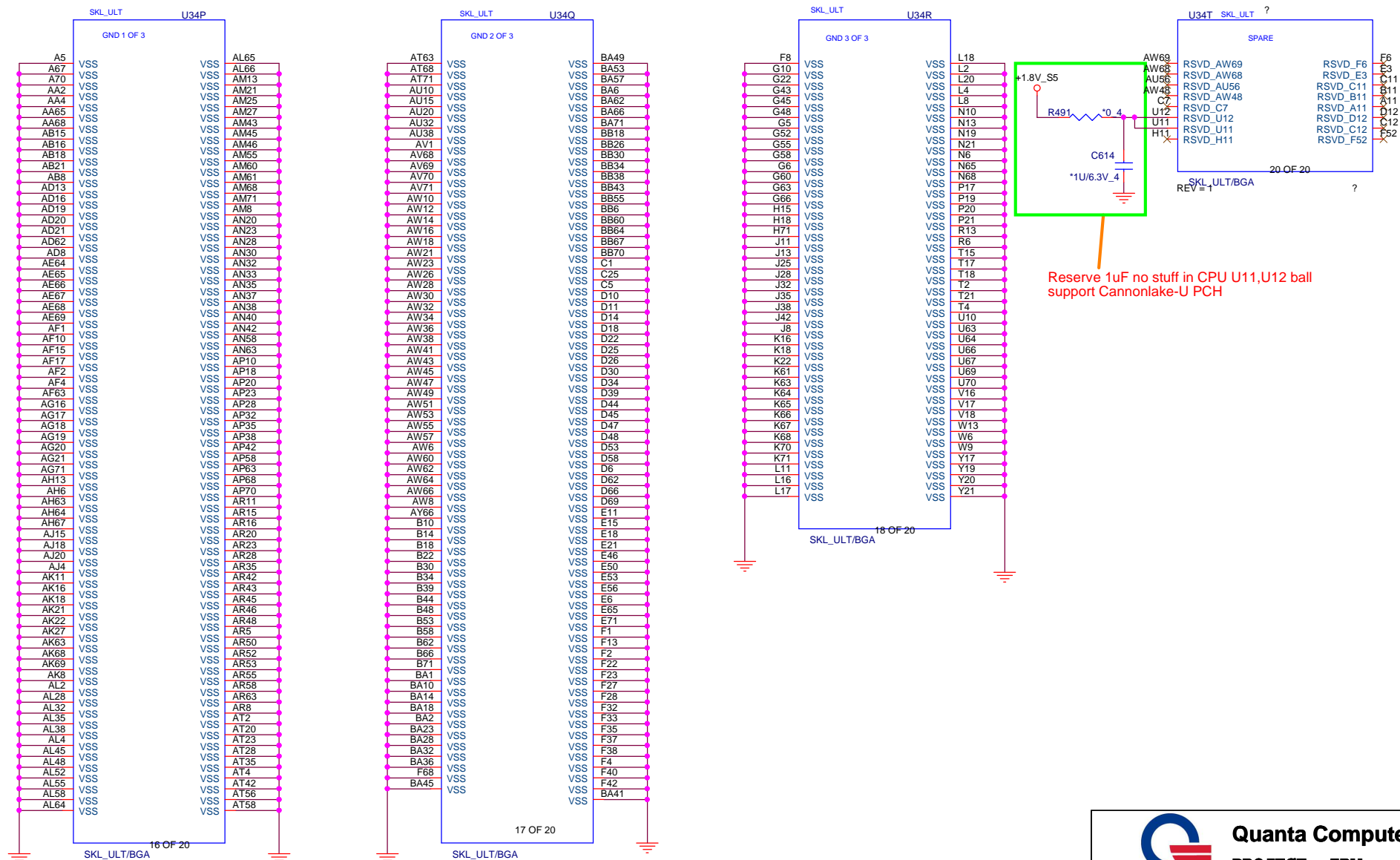


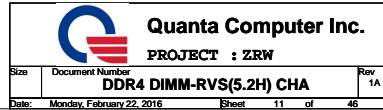
## PLTRST# Buffer

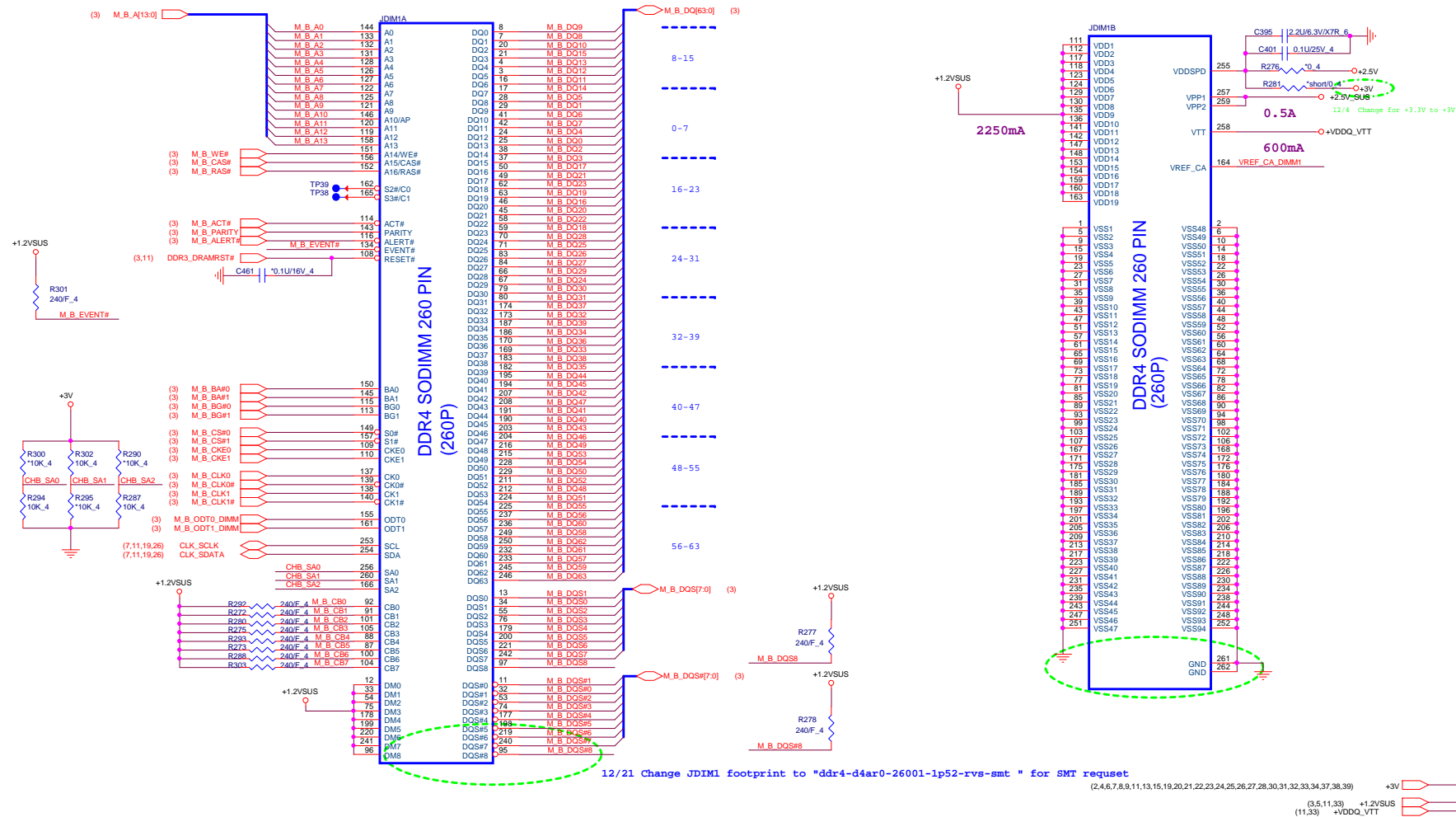


A

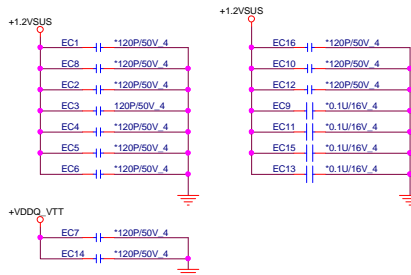
## Skylake ULT (GND)





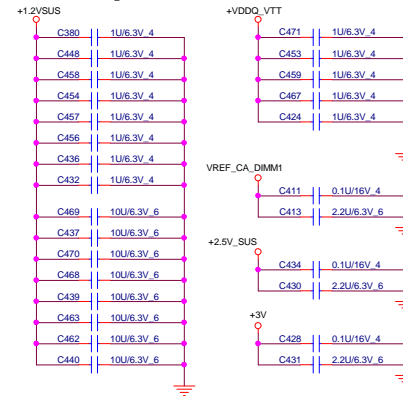


## For EMI RESERVE

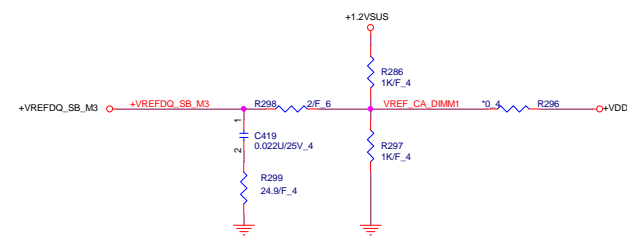


## Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



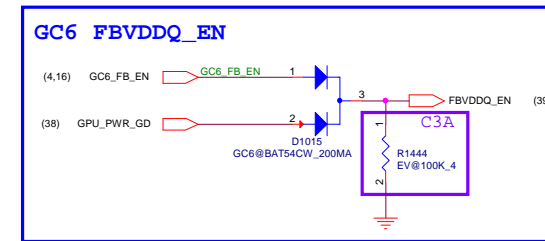
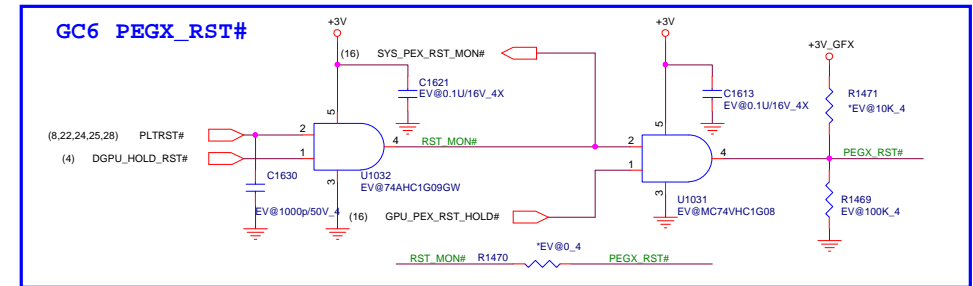
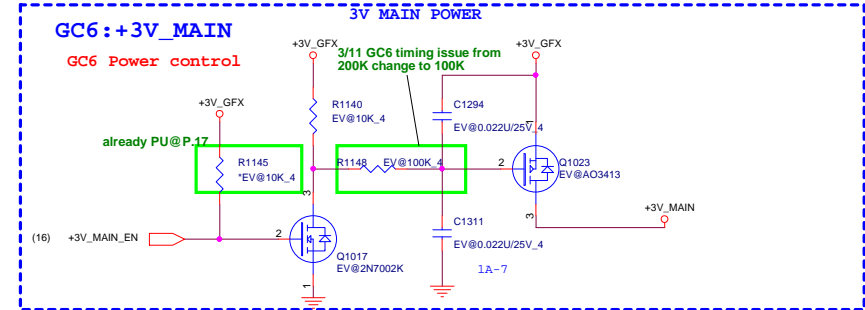
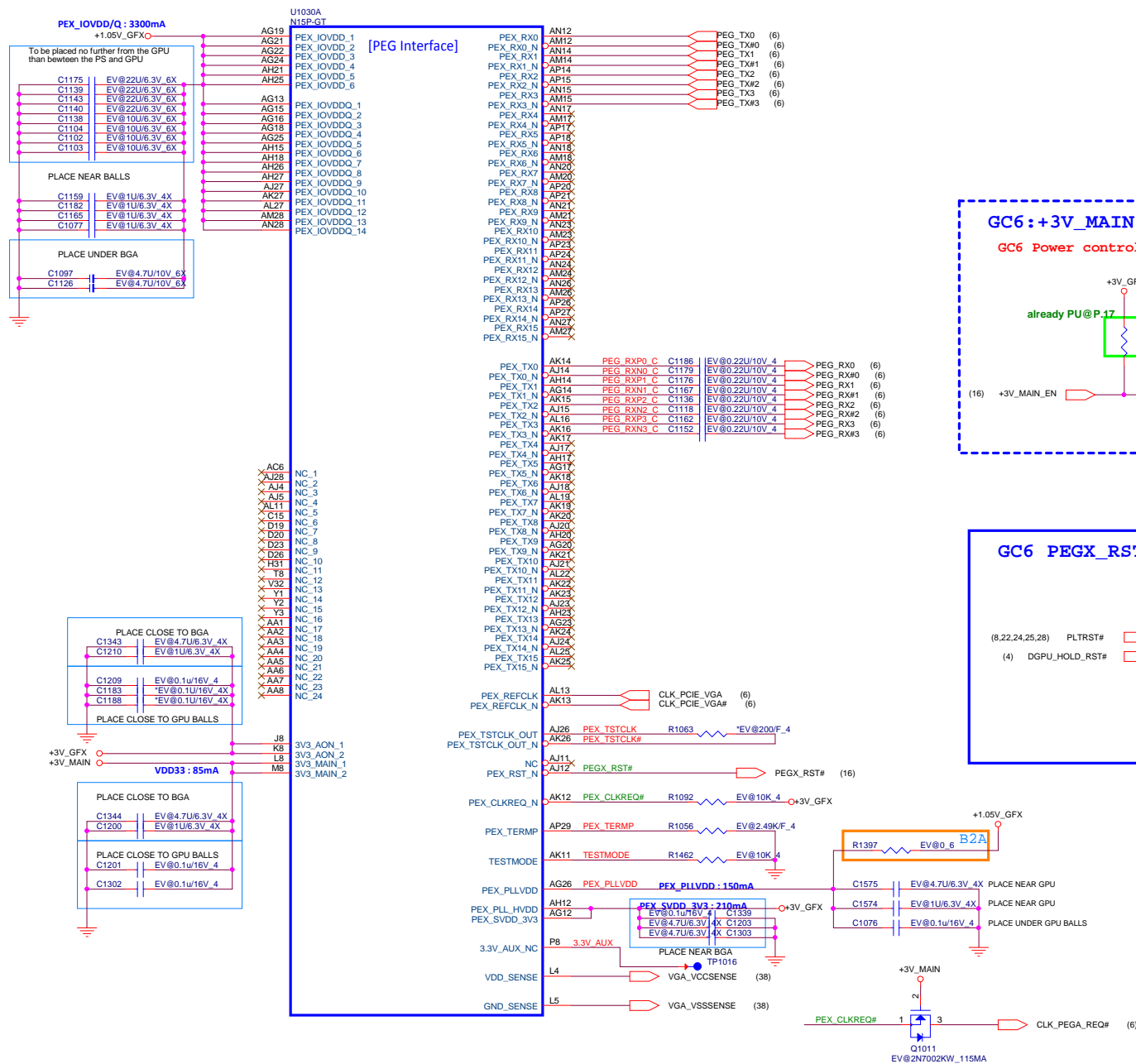
## VREF DQ1 M1 Solution

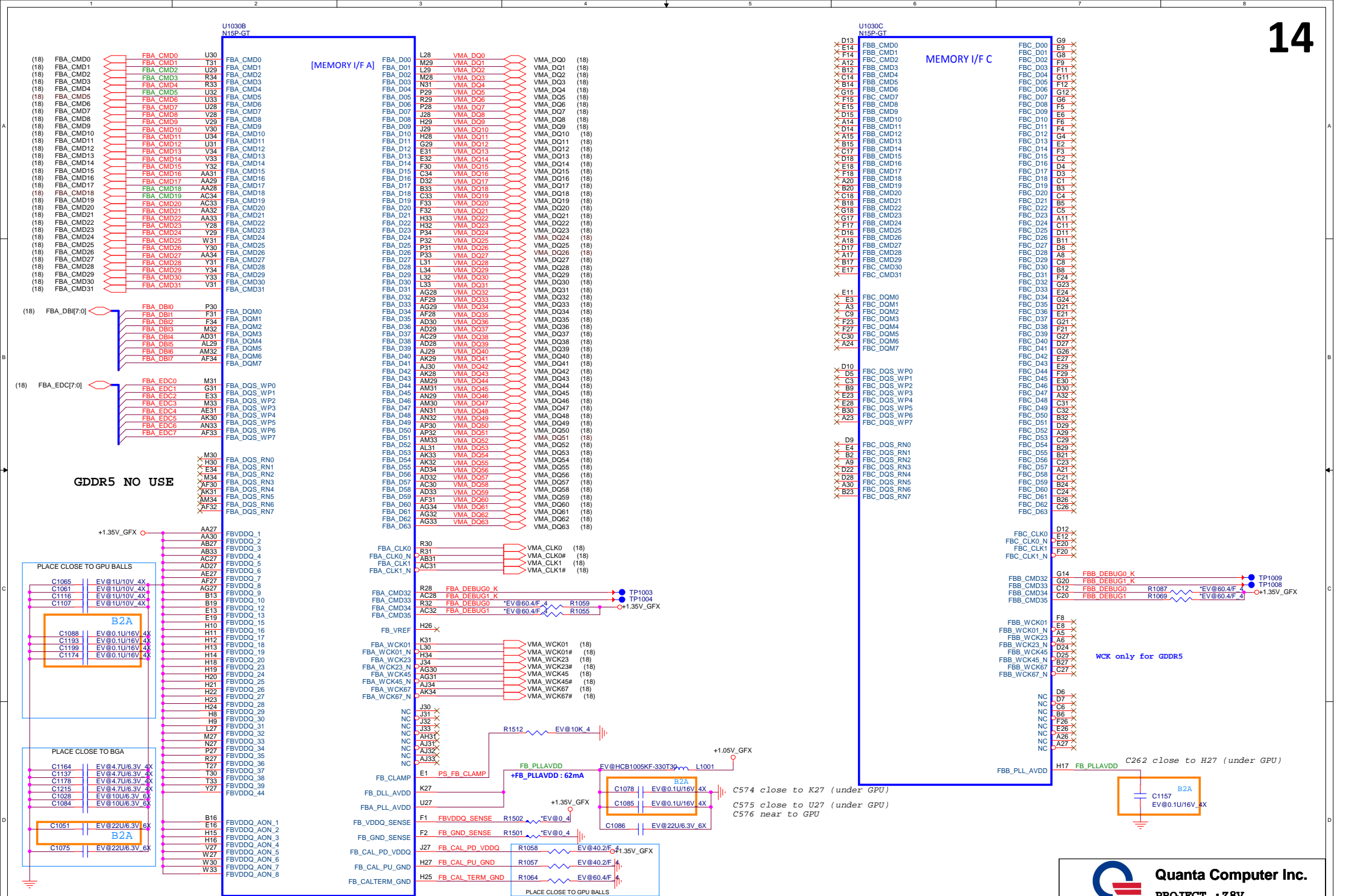


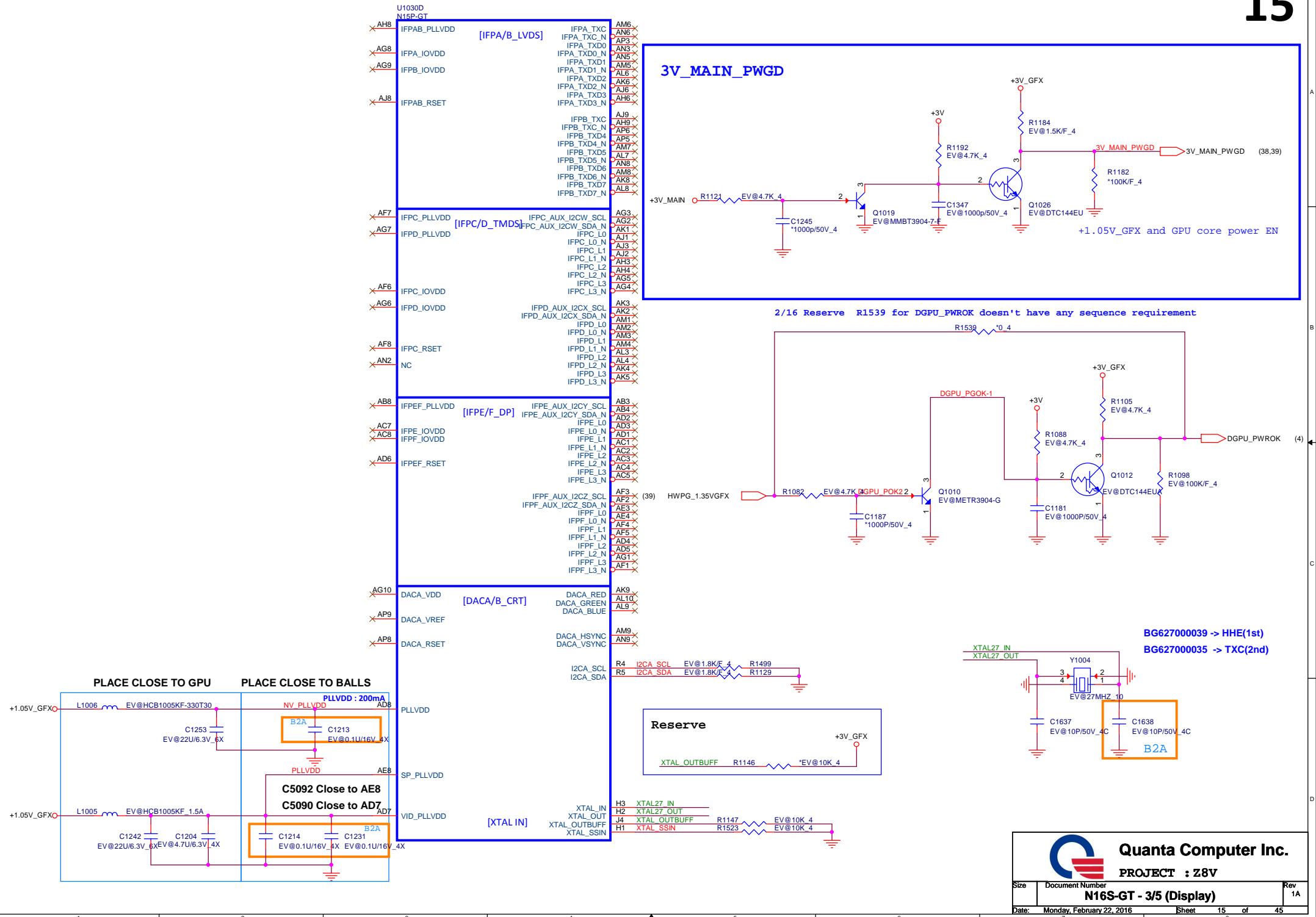
Quanta Computer Inc.

PROJECT : ZRW

Size	Document Number	Rev
	DDR4 DIMM-STD(5.2H) CHB	1A
Date:	Monday, February 22, 2016	Sheet 12 of 46





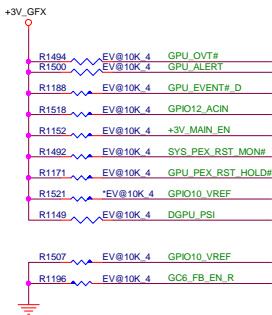


Resistor P/N  
 4.99K → CS24992FB26  
 10K → CS31002FB26  
 15K → CS31502FB24  
 20K → CS32002FB29  
 24.9K → CS32492FB16  
 30.1K → CS33012FB18  
 34.8K → CS33482FB22  
 45.3K → CS34532FB18 GM  
 49.9K → CS34992FB10 GT

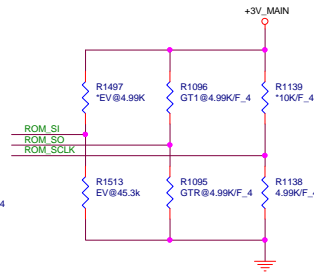
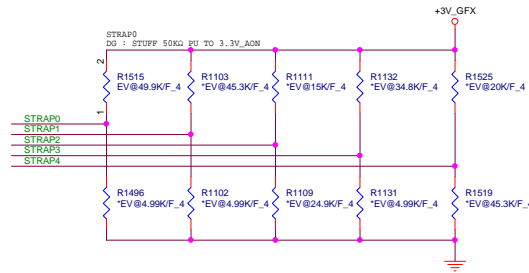
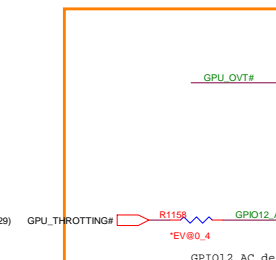
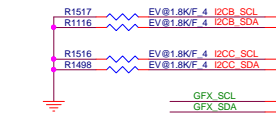
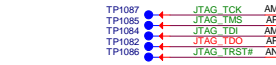
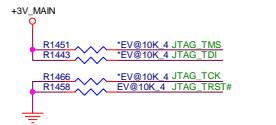
U1030E  
 N16S-GT

[MIOA]

[MIOB]



Reserve PU/PD for Debug



	PU +3V_MAIN	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Mutil-level mode strapping:

For N16S-GT1-KB-A2 :

- R490=40.2K PD
- ROM\_SO = 4.99K PU (N16S-GTR = 4.99KPD)
- ROM\_SI = Memory strap setting
- STRAP0 = 49.9K PU
- Strap4~1 = Reserve Pull up and Pull down

	N16S-GT1-KB-A2	N16S-GTR
ROM_SO	R93 PU 4.99K	R92 PD 4.99K
ROM_SI	As below configuration table	

N16S-GT1-KB-A2 VRAM Configuration Table:

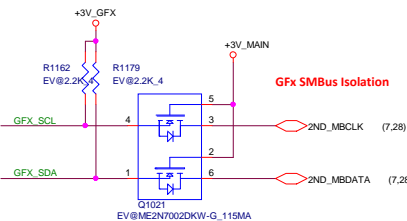
	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GDDR5 128MBx32,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GDDR5 256MBx16,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x0) 0001 (0x1)	GDDR5 256MBx32,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDTS02 AKG5LGUTL04	4.99K Pull up 10K Pull up
8GbX4 (4GB)	0000 (0x0) 0001 (0x1)	GDDR5 512MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDTS02 AKG5LGUTL04	4.99K Pull up 10K Pull up

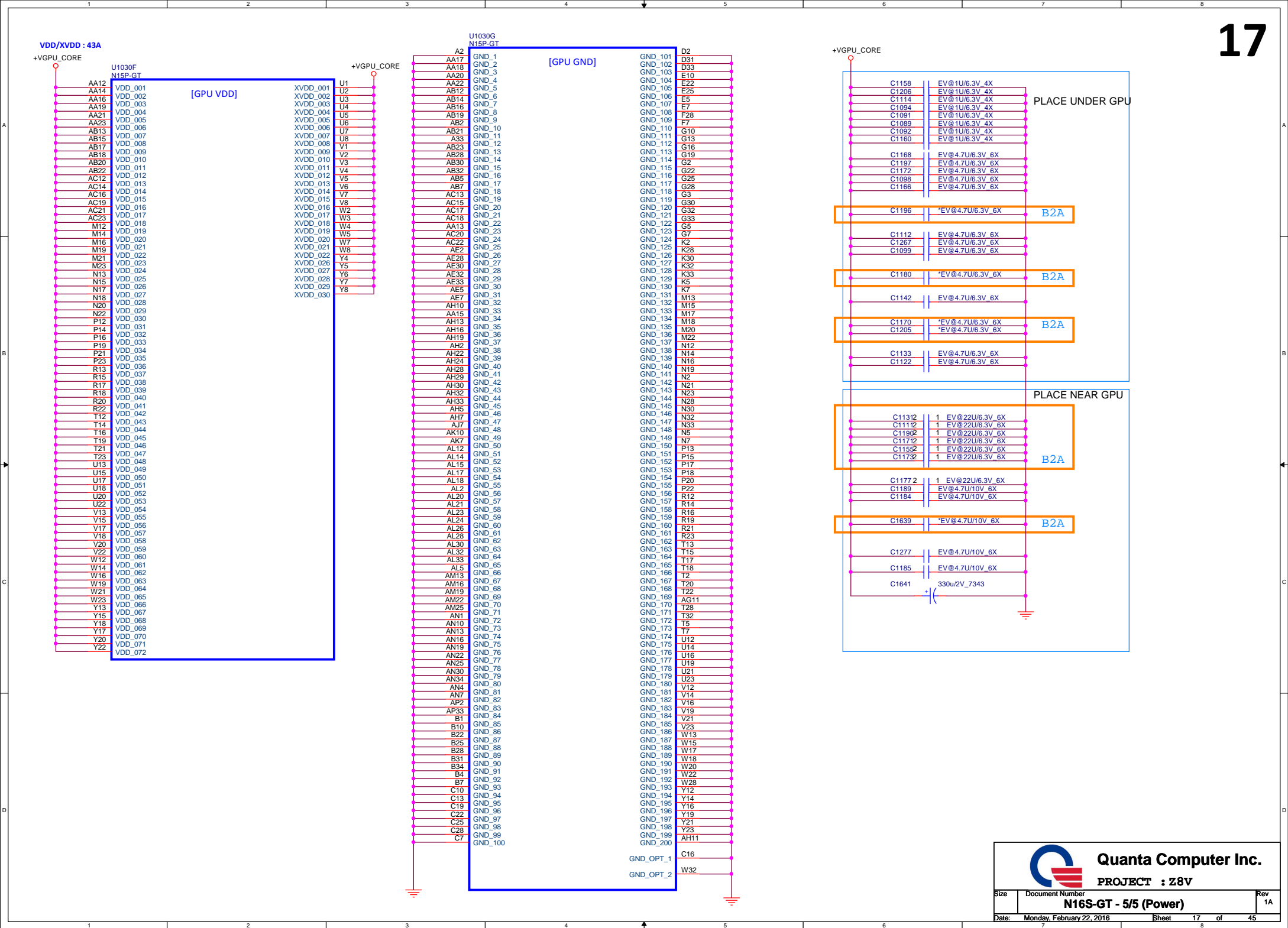
N16S-GTR VRAM Configuration Table:

	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GDDR5 128MBx32,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GDDR5 256MBx16,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x0) 0001 (0x1)	GDDR5 256MBx32,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDTS02 AKG5LGUTL04	4.99K Pull down 10K Pull down
8GbX4 (4GB)	0000 (0x0) 0001 (0x1)	GDDR5 512MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDTS02 AKG5LGUTL04	4.99K Pull down 10K Pull down

N16S-GT1-KB-A2 (GB4b-128)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep footprint to PU to 3V3_AON and PD to GND [Stiff 49.9K PU]			
STRAP1	Keep footprint to PU to 3V3_AON and PD to GND [Do Not Stiff]			
STRAP2				
STRAP3				
STRAP4				





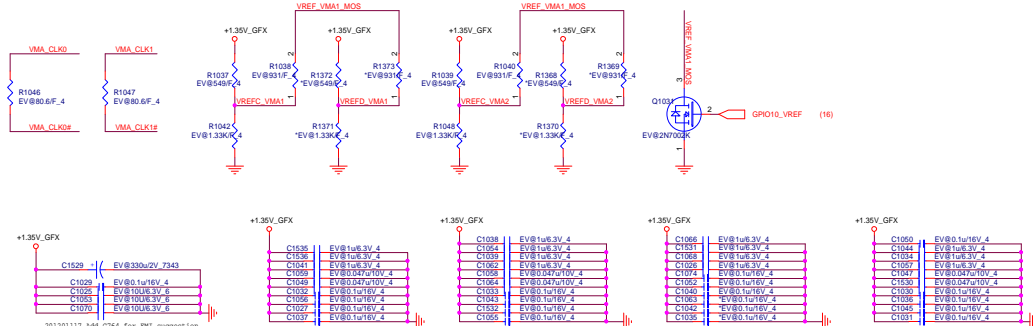
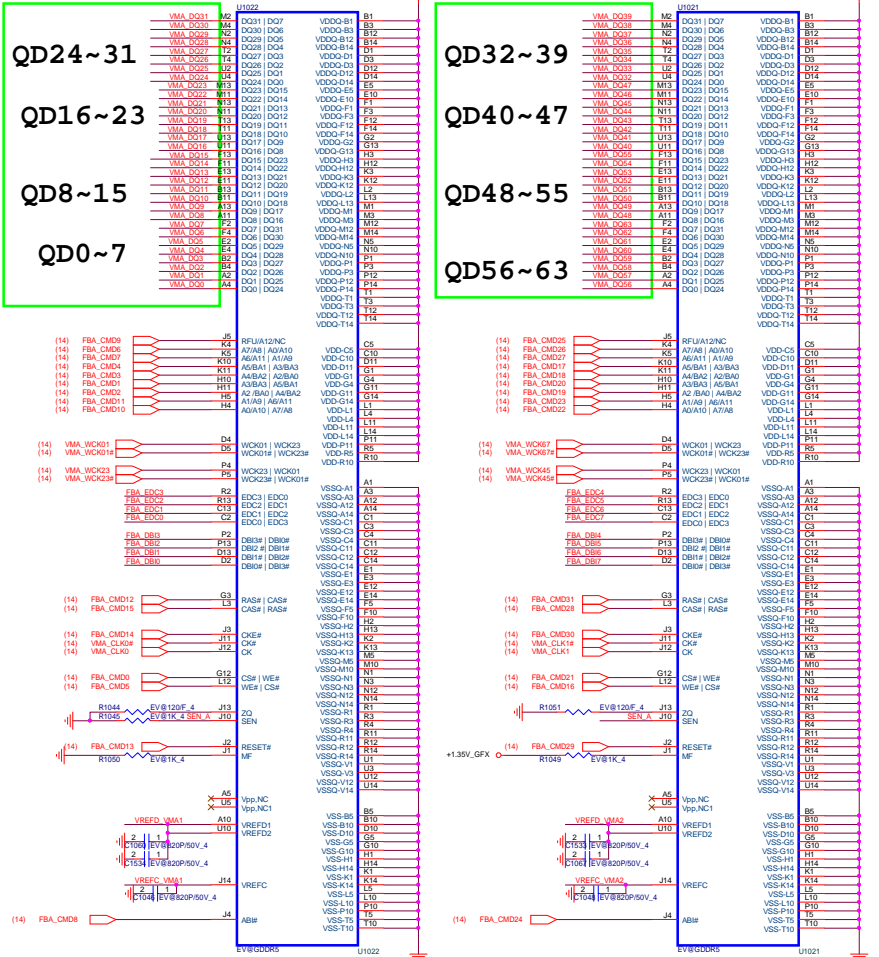
Channel 0  
<0-31>

LOWER HALF

Channel 0  
<32-63>

MF=0 Non-mirrored

MF=1 mirrored



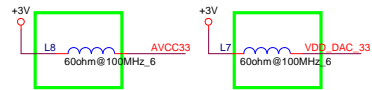
## GDDR5 Mode II Mapping

Channel	Bank	Memory
0	0	0
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14
15	15	15
16	16	16
17	17	17
18	18	18
19	19	19
20	20	20
21	21	21
22	22	22
23	23	23
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27	27	27
28	28	28
29	29	29
30	30	30
31	31	31

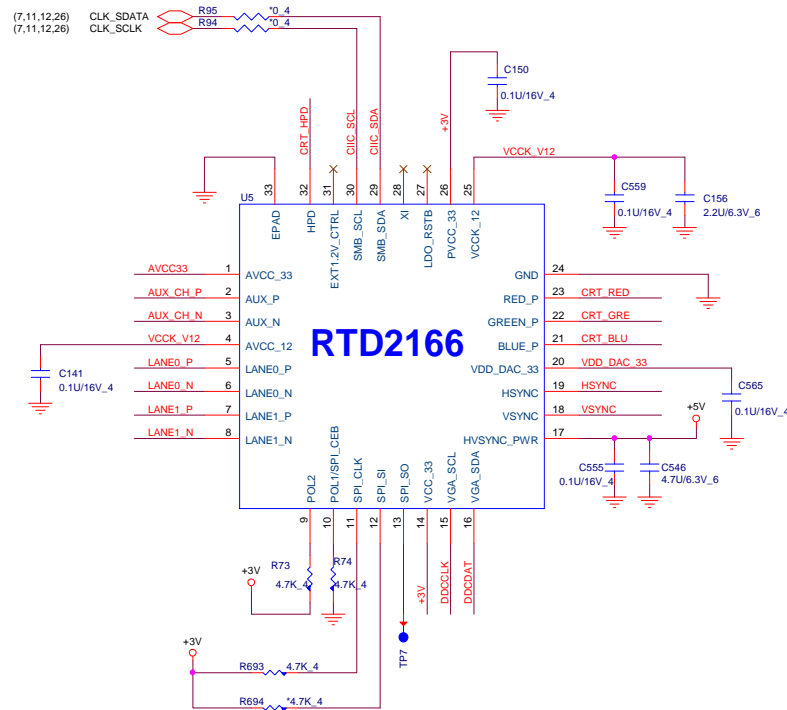
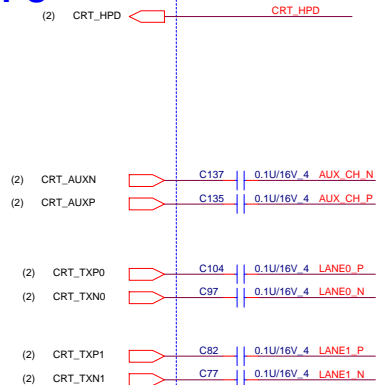
RST PD place @ the end of daisy-chain.

## DP TO VGA

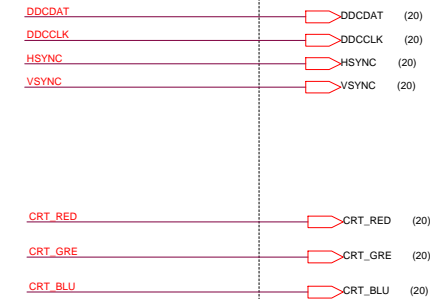
## Power



## CPU



## VGA



## Note:

- 1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
- 2- C5 should be X5R material
- 3- R6, R7, R8 should be 75 ohm with +/-1%
- 4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
- 5- This configuration is for internal ROM mode and using embedded LDO mode.

(2,4,6,7,8,9,11,12,13,15,20,21,22,23,24,25,26,27,28,30,31,32,33,34,37,38,39) +3V  
(20,21,23,24,26,30,37) +5V



HDMI <HDM>

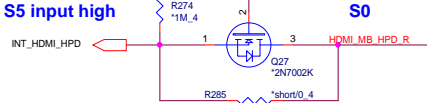
OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

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Inputs		Equalization for 3 Gbit/s
EQ1		
short to GND	short to GND	0 dB
short to GND	short to Vpp	2 dB
short to Vpp	short to GND	4 dB
short to Vpp	short to Vpp	6 dB

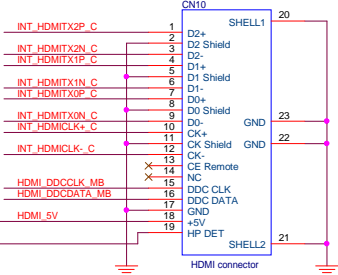
From PCH

HDMI-detect

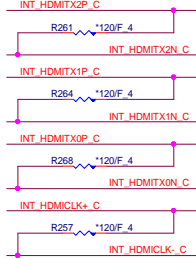


DDS AL002331000

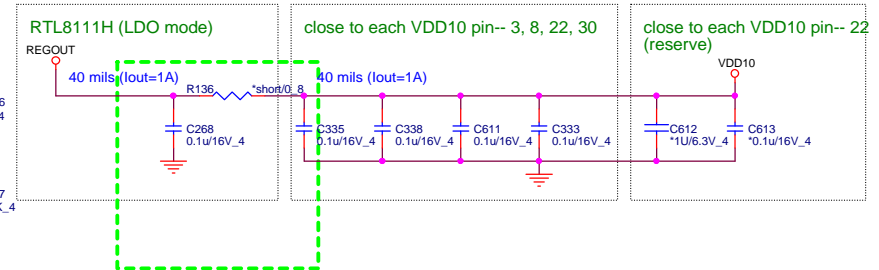
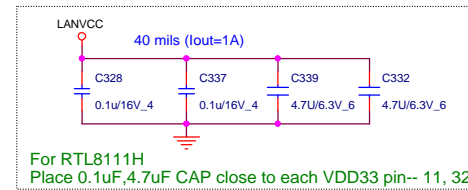
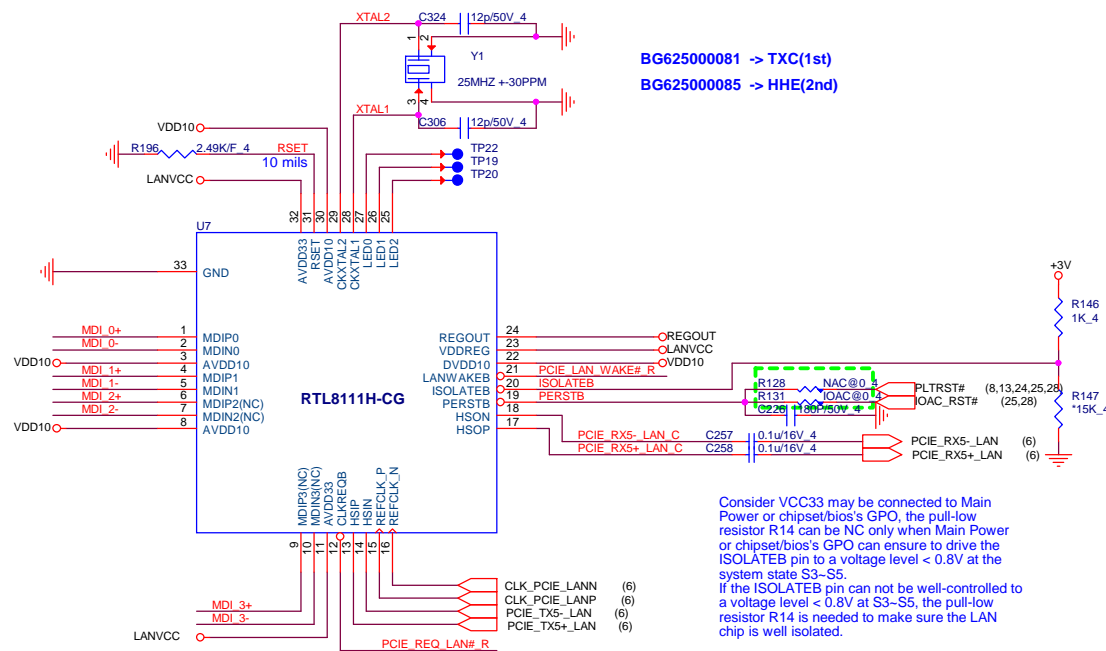
HDMI connector



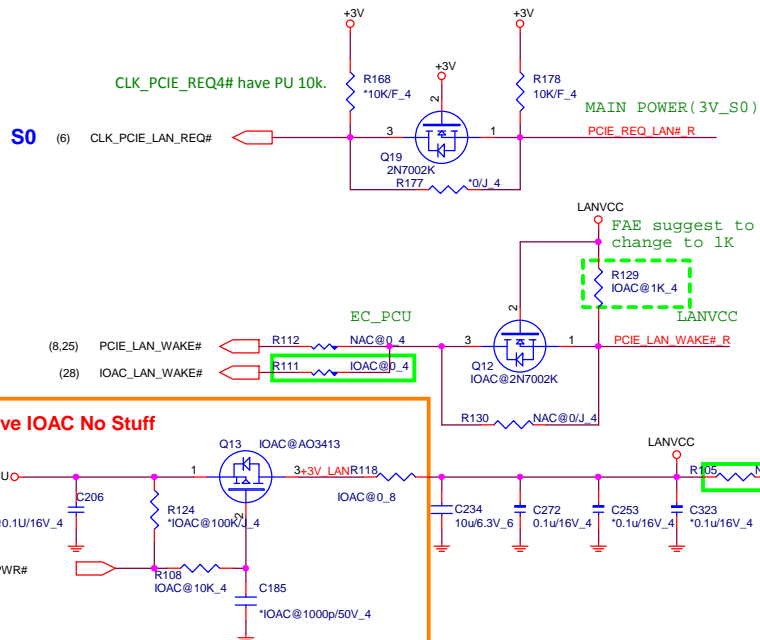
EMI



Power trace tracking

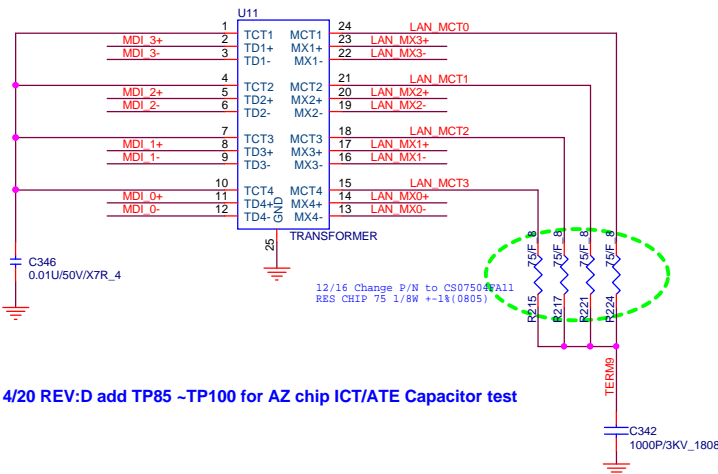


## Leakage circuit (MPC)

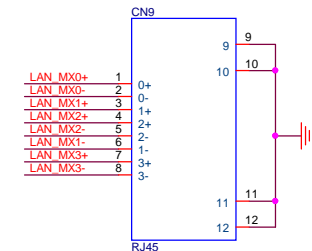


## Transformer

Layout: All termination signal should have 30 mil trace

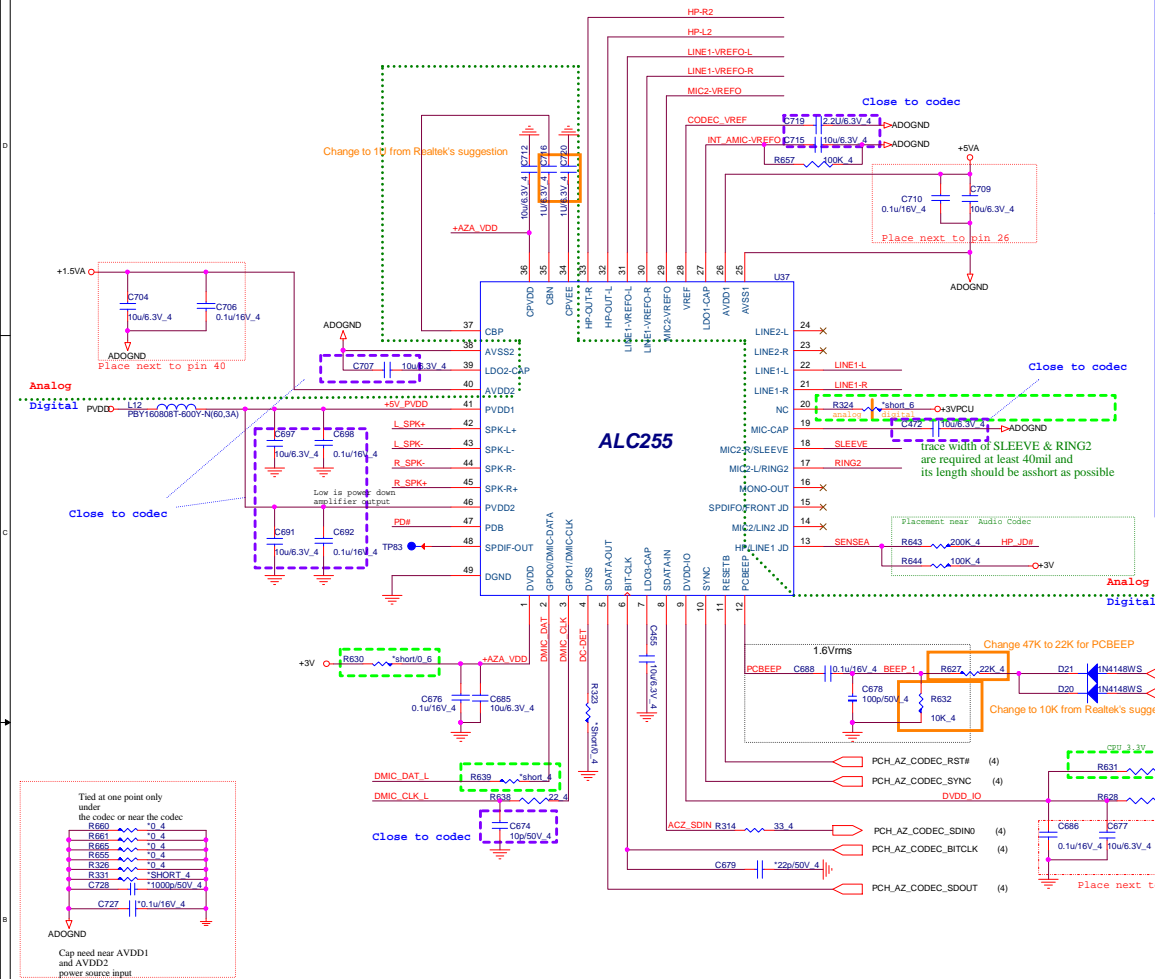


## RJ45 Connector

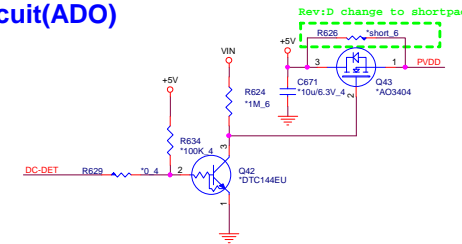


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 PROJECT : ZRW

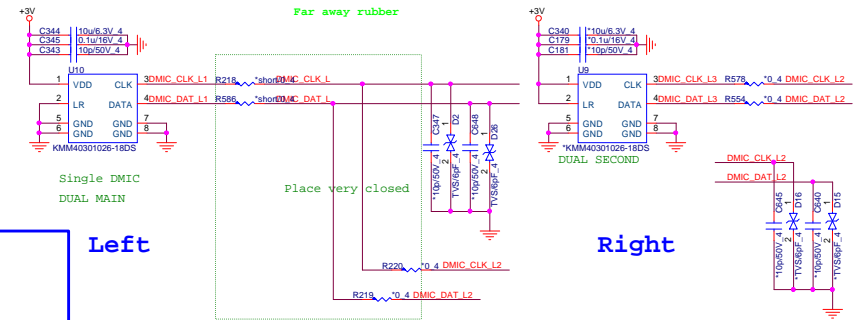
## Codec(ADO)



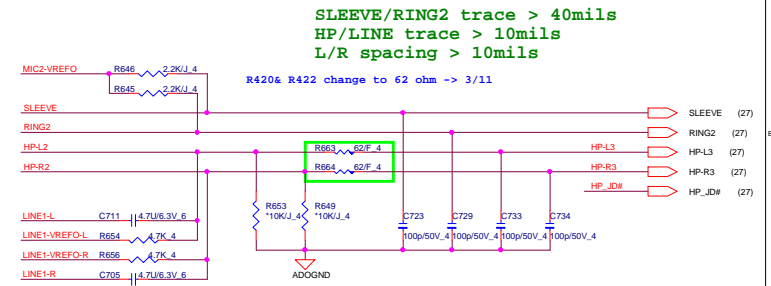
## DC-DET circuit(ADO)



## D-Mic (MIC)



## Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

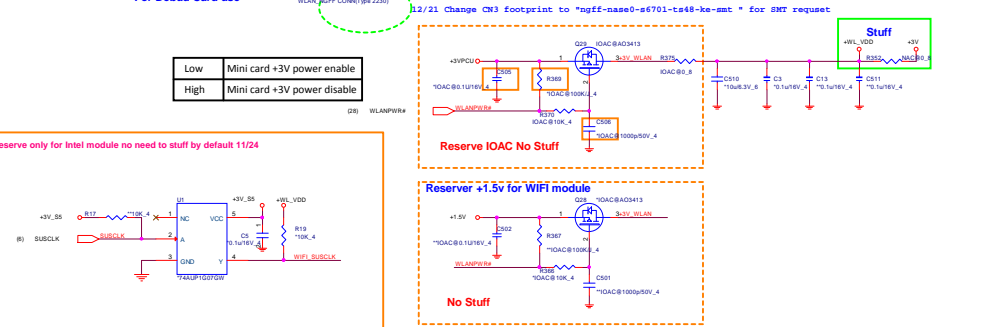
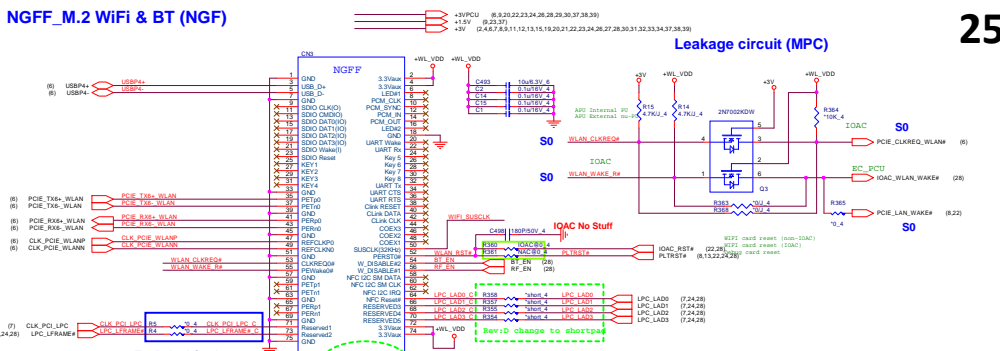


20120921 change Cn10 Pin define following Z09.

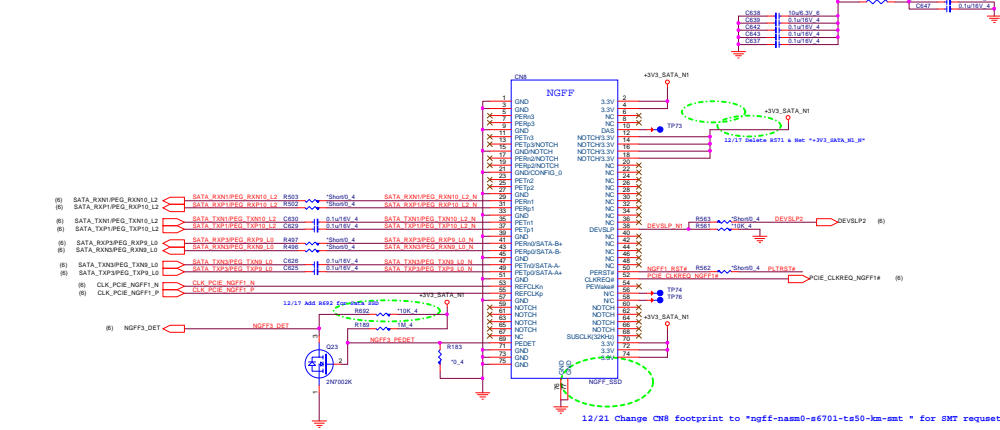


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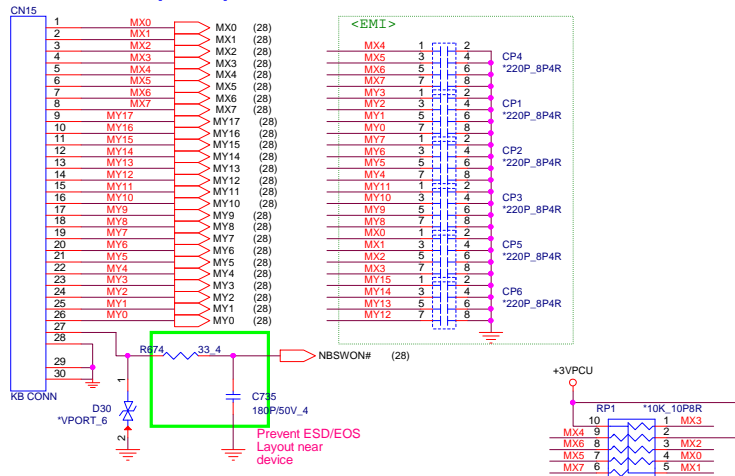




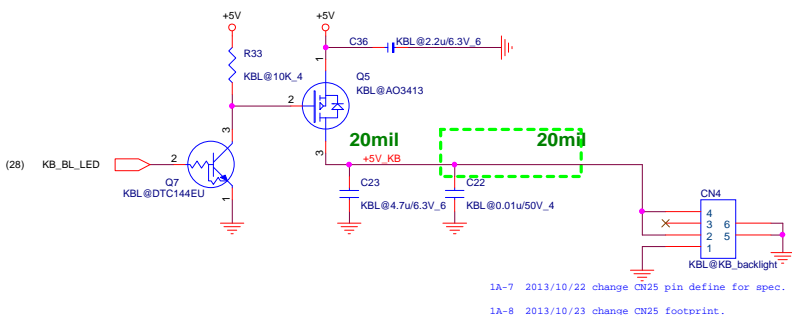
NGFF\_M.2 SSD (NGF)



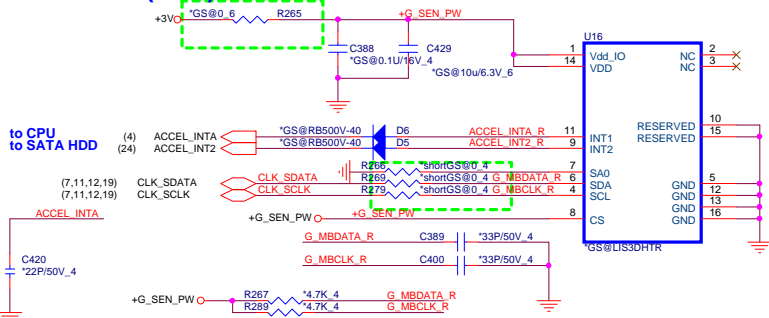
## KEYBOARD (KBC)



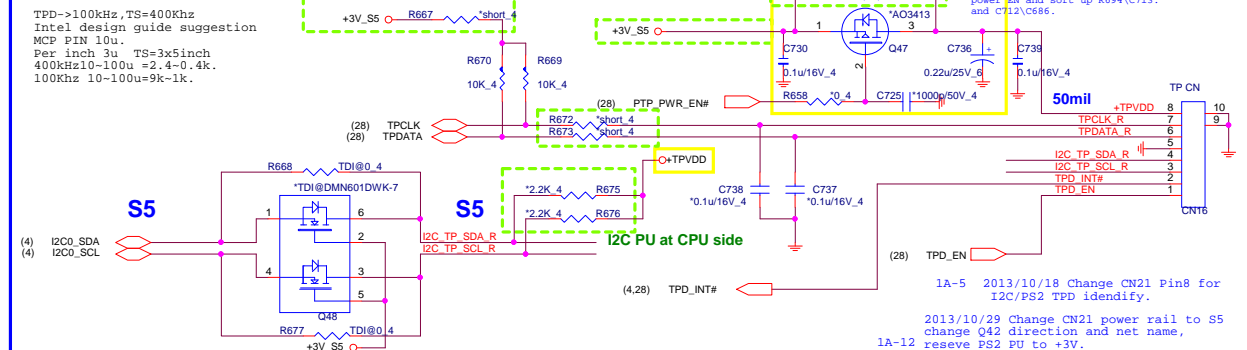
## KB\_LED (KBC)



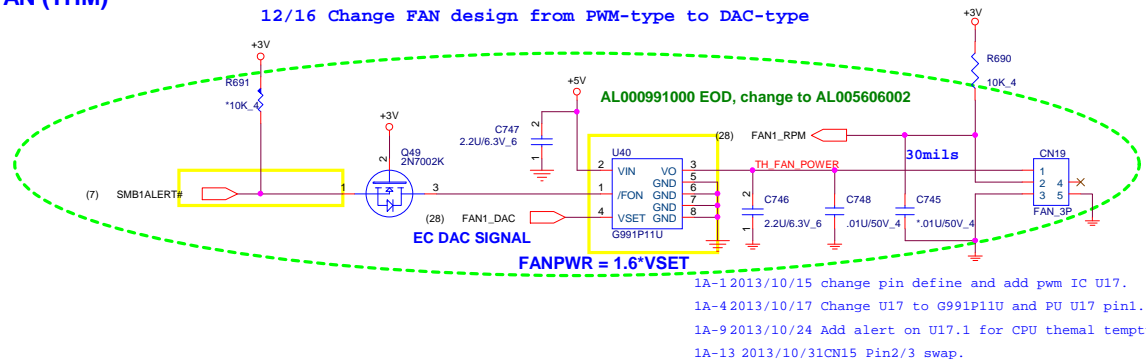
## G-sensor(ACS)



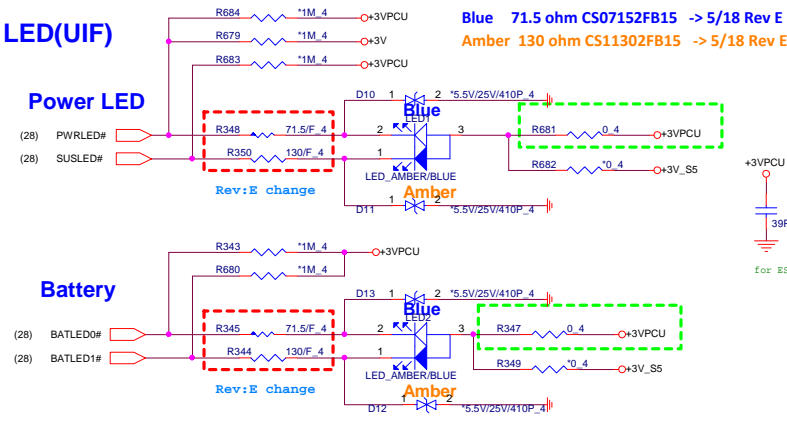
## TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



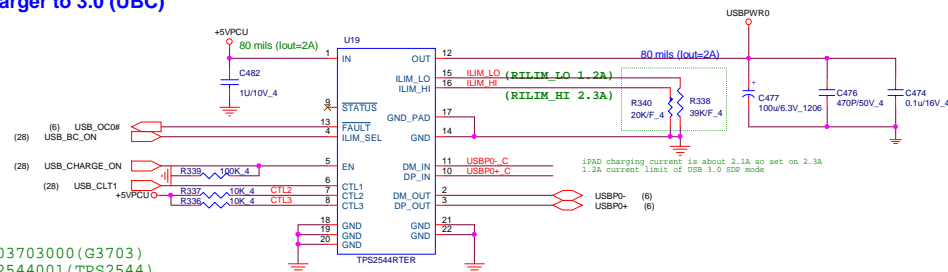
## CPU FAN (THM)



## POWER LED(UIF)



## USB Charger to 3.0 (UBC)



GMT:AL003703000(G3703)  
 TI:AL002544001(TPS2544)  
 Silergy: AL055544000 (SLGC55544VTR)

	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

ILIM\_LO is optional and the ILIM\_LO pin may be left unconnected if the following conditions are met:

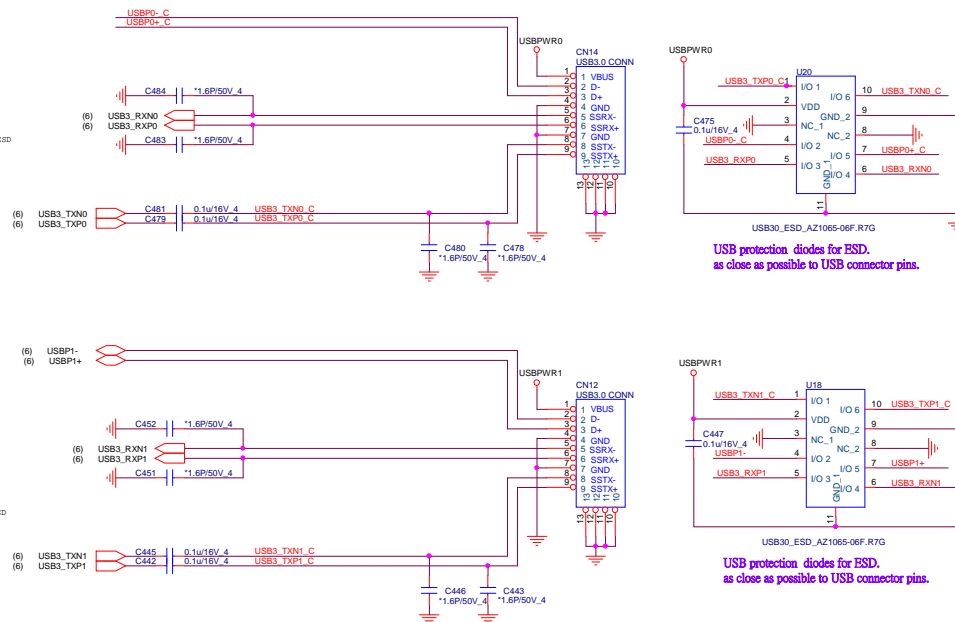
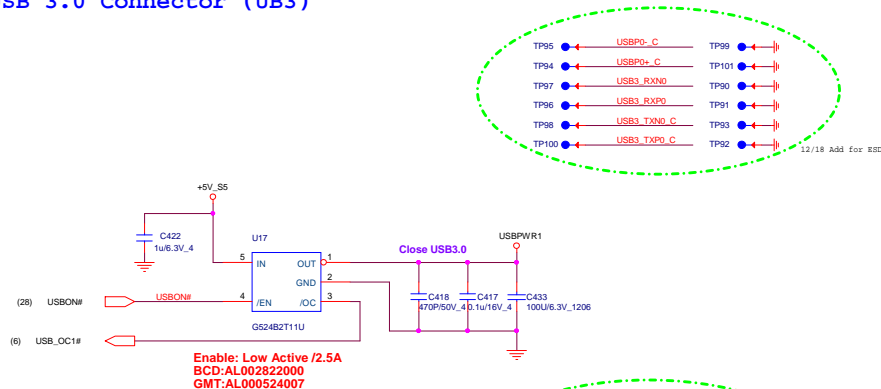
1. ILIM\_SEL is always set high
  2. Load Detection - Port Power Management is not used
  3. Mouse / Keyboard wake function is not used
- If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use ILIM\_LO < 80.6 kΩ.

The following equation programs the typical current limit:

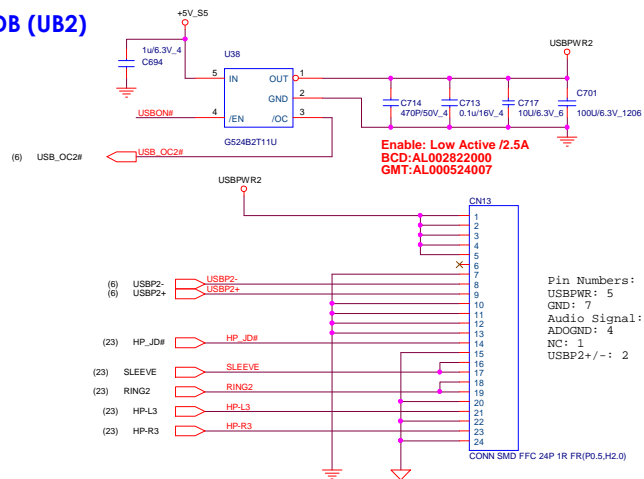
(1)  
 ILIM\_XX corresponds to either RILIM\_HI or RILIM\_LO as appropriate.

$$I_{OS\_typ}(mA) = 50,250 / \{RILIM\_XX(K\Omega) + 0.1\}$$

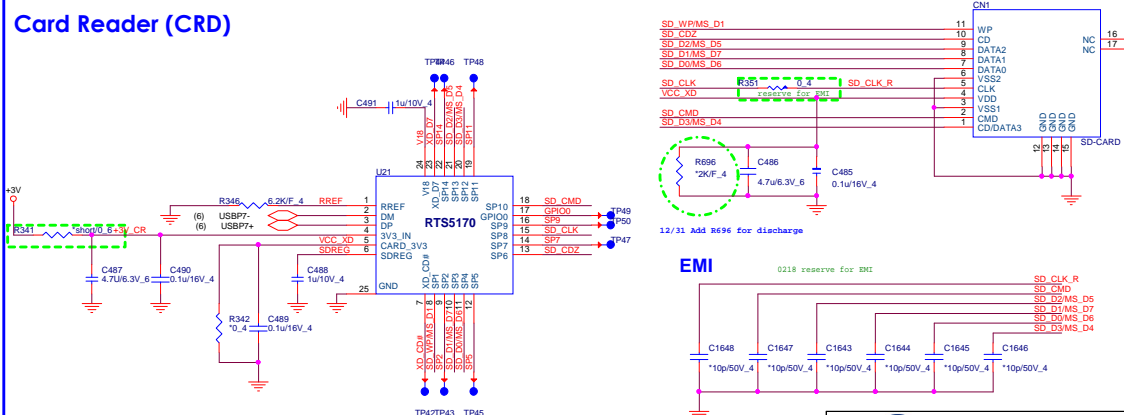
## USB 3.0 Connector (UB3)



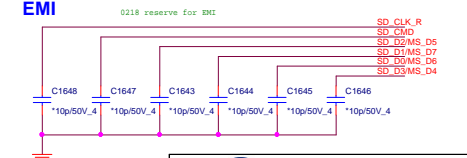
## USB2.0 DB (UB2)

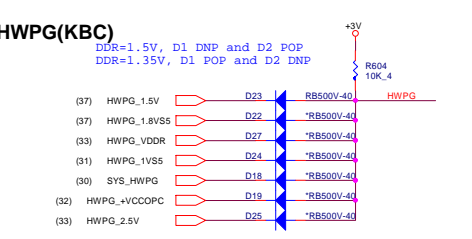
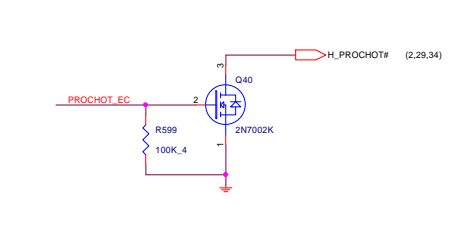
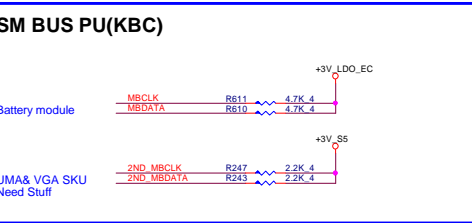
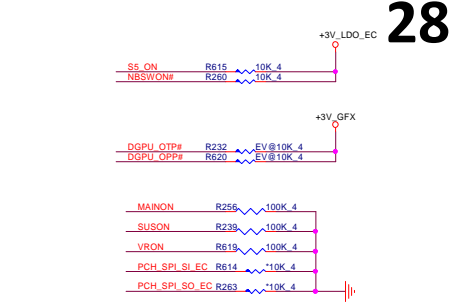
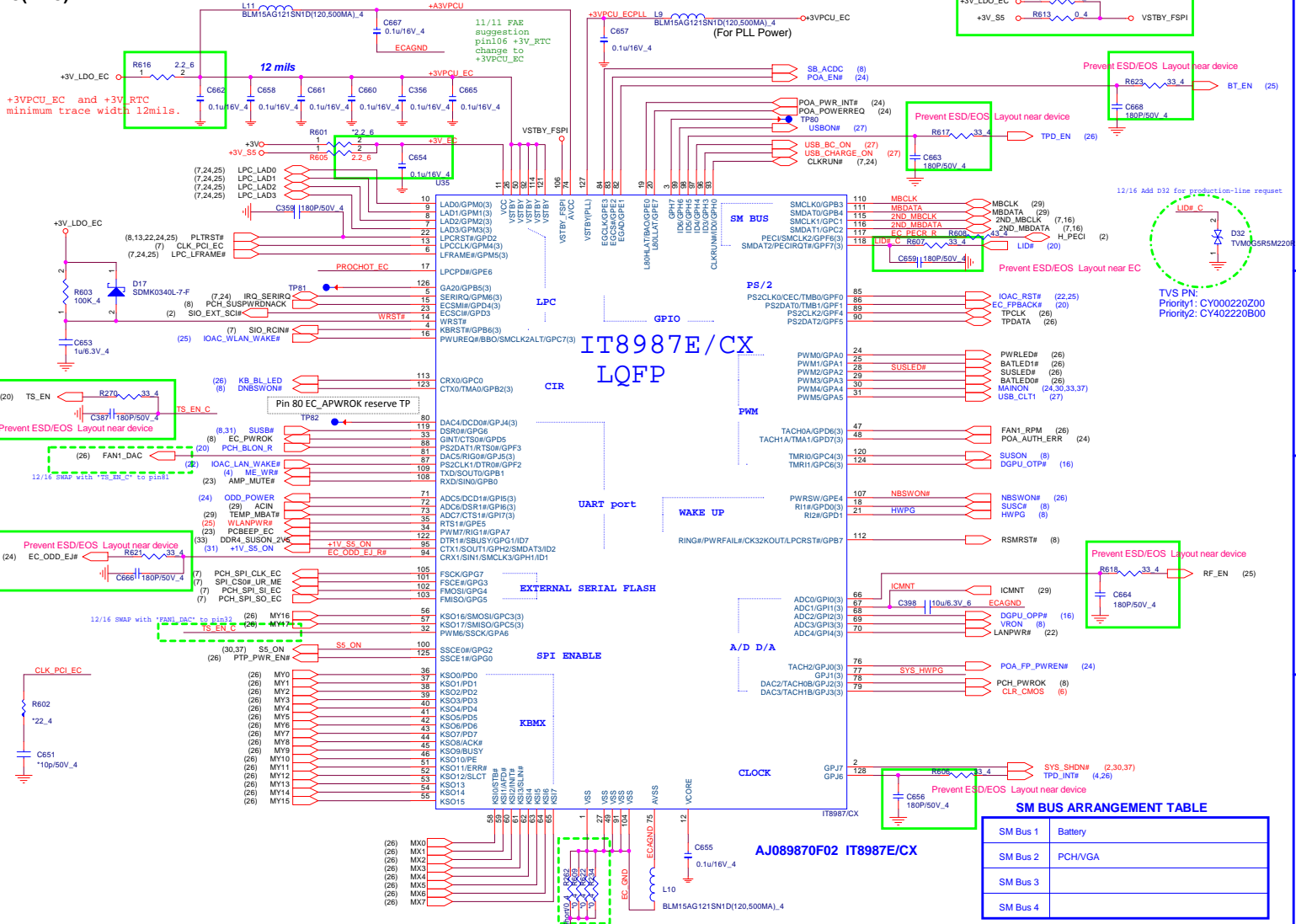


## Card Reader (CRD)

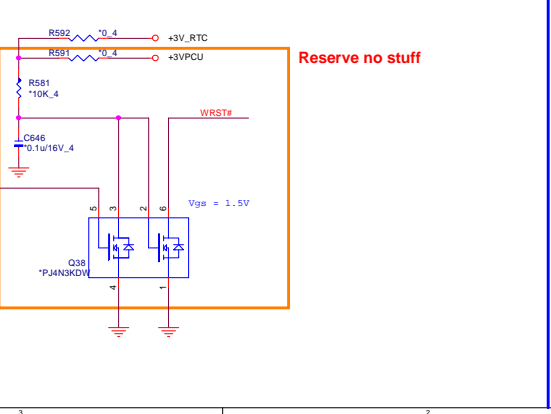
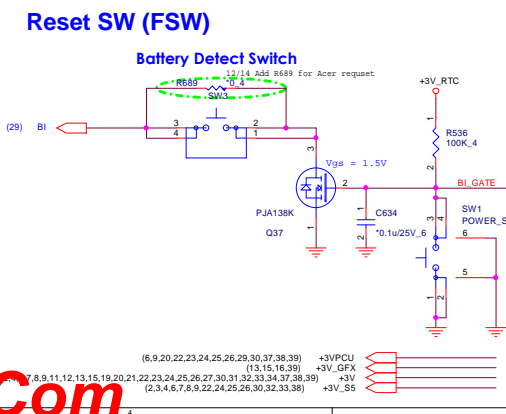
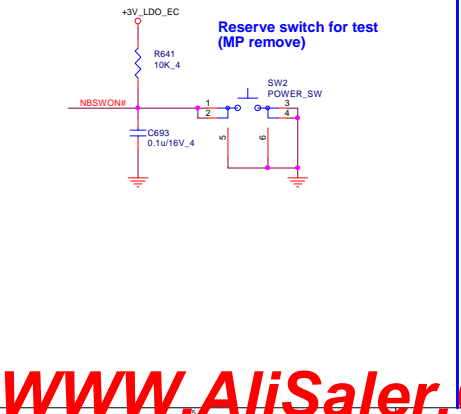


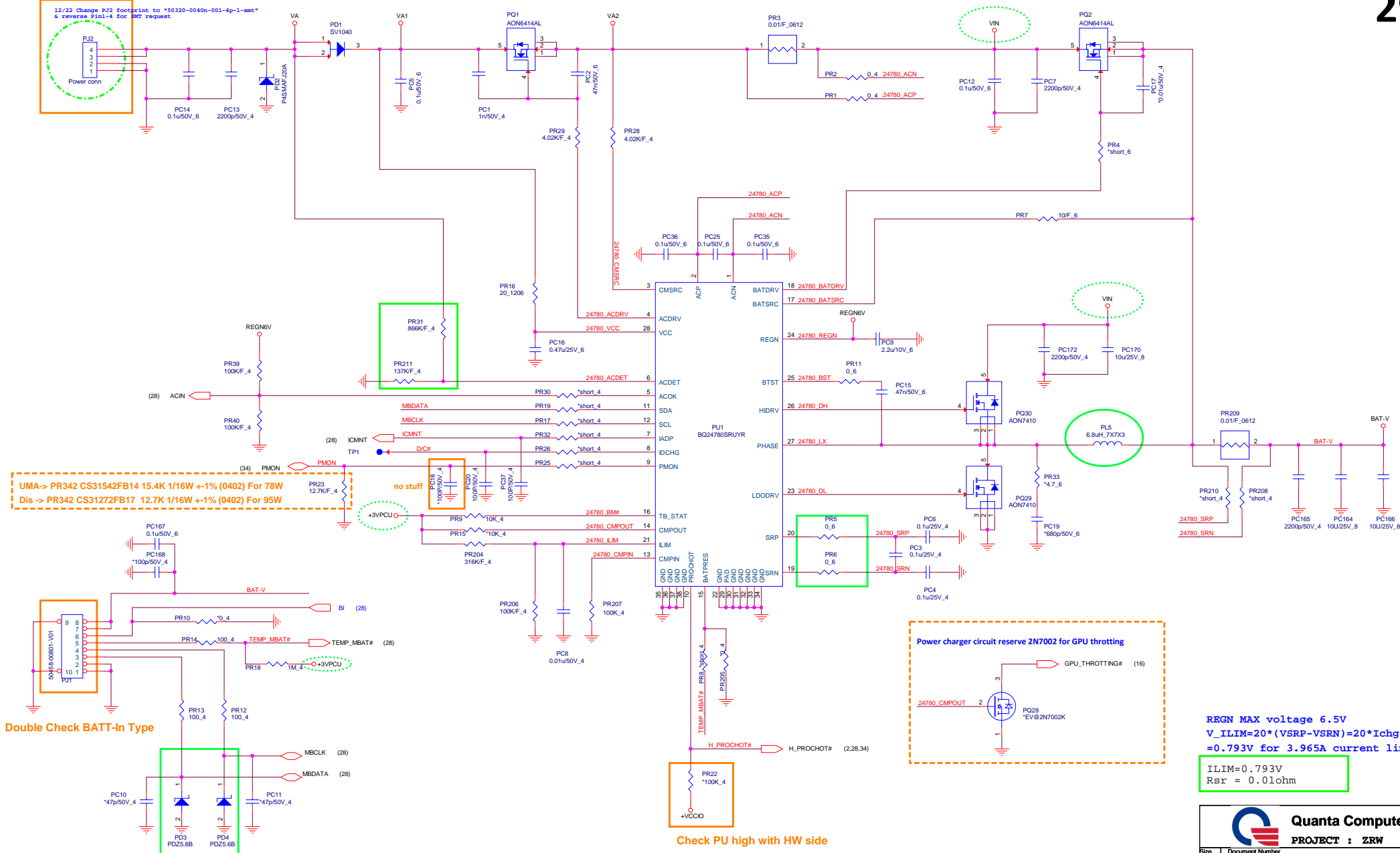
EMI

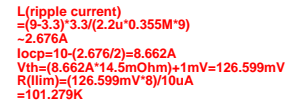


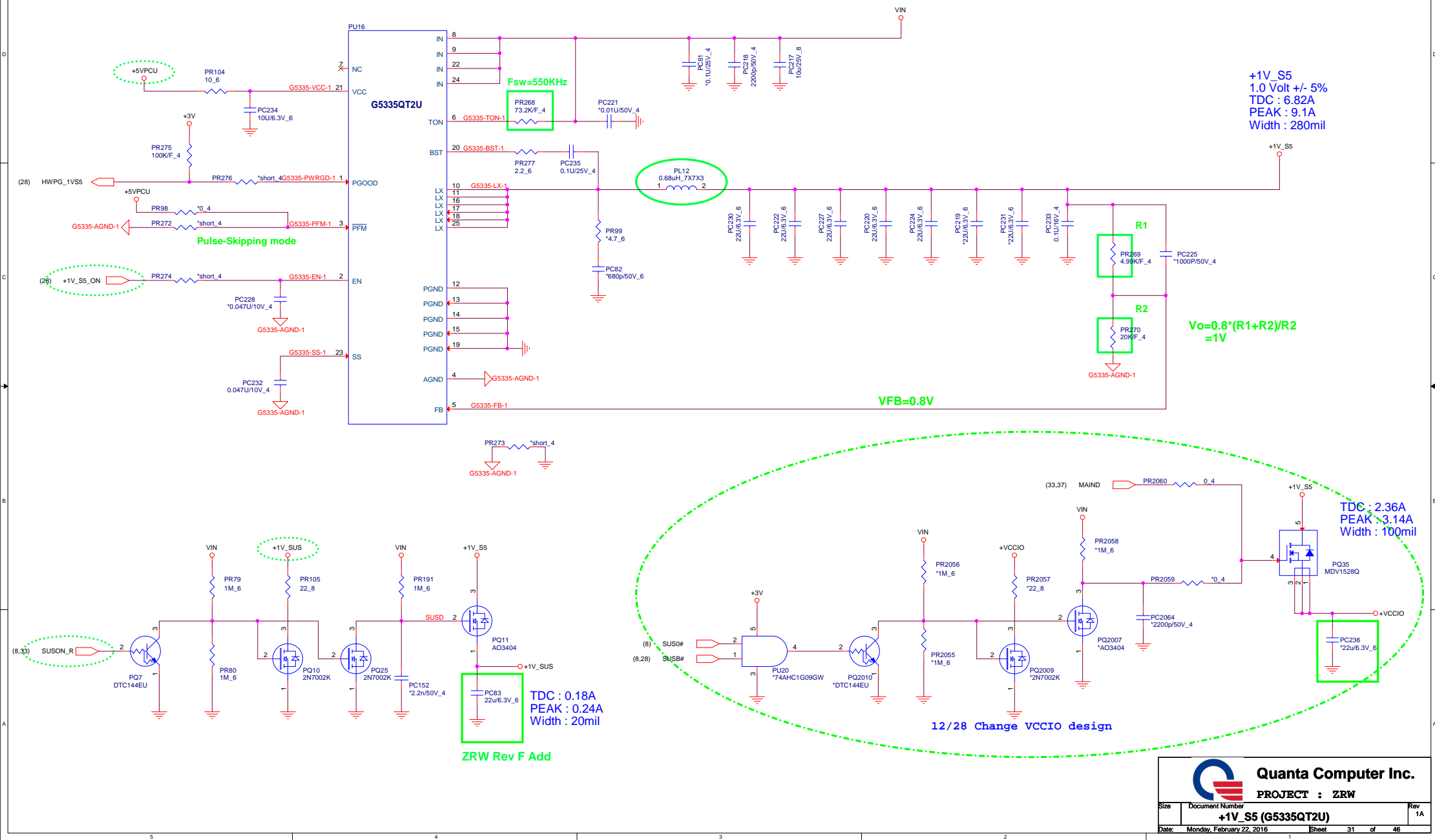


SM BUS ARRANGEMENT TABLE	
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	









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## +VCCOPC Power only for 2+3e CPU

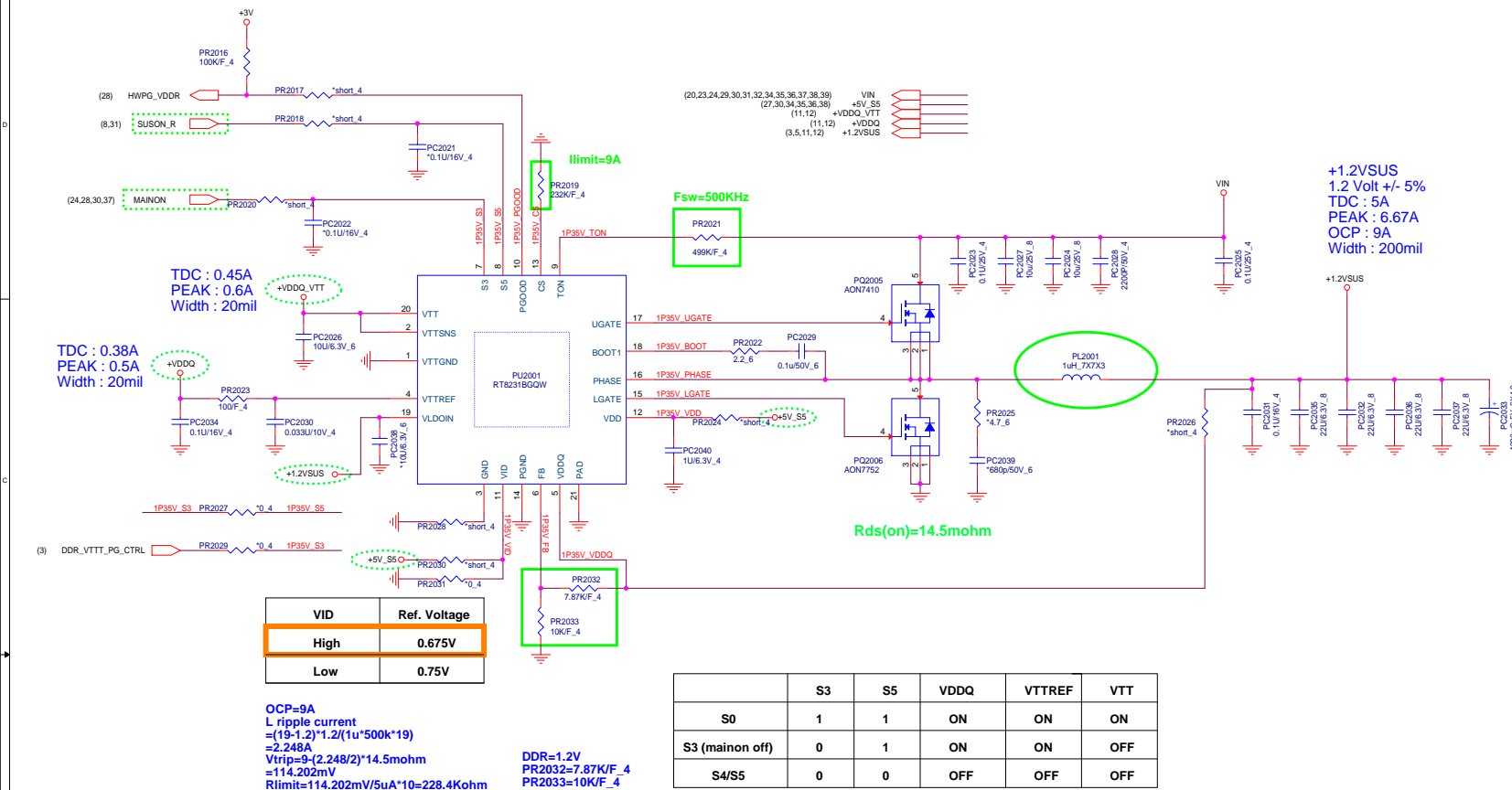
+VCCOPC  
TDC : 4.5A  
PEAK : 6A  
Width : 200mil

Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIC
150K	Other

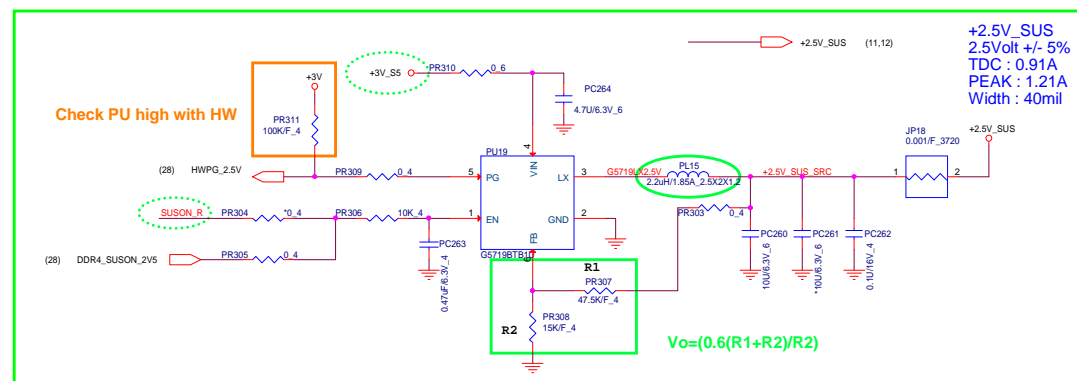
	LP#	C1	C0	Vo
<b>VCCEDRAM</b>	0	X	X	0V
	1	0	0	0.8V(MSM)
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V

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**PROJECT : ZRW**

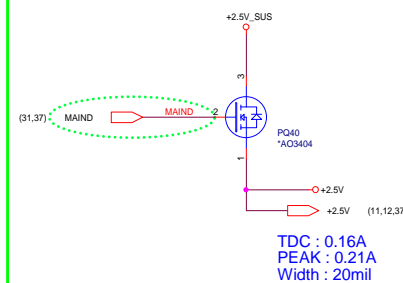
(5) +VCCOPC → (20,23,24,29,30,31,33,34,35,36,37,38,39)  
VIN → (2,4,6,7,8,9,11,12,13,15,19,20,21,22,23,24,25,26,27,28,30,31,33,34,37,38,39)  
+3V → (2,3,4,6,7,8,9,22,24,25,26,28,30,33,38)  
+3V\_S5 → (2,3,4,6,7,8,9,22,24,25,26,28,30,33,38)



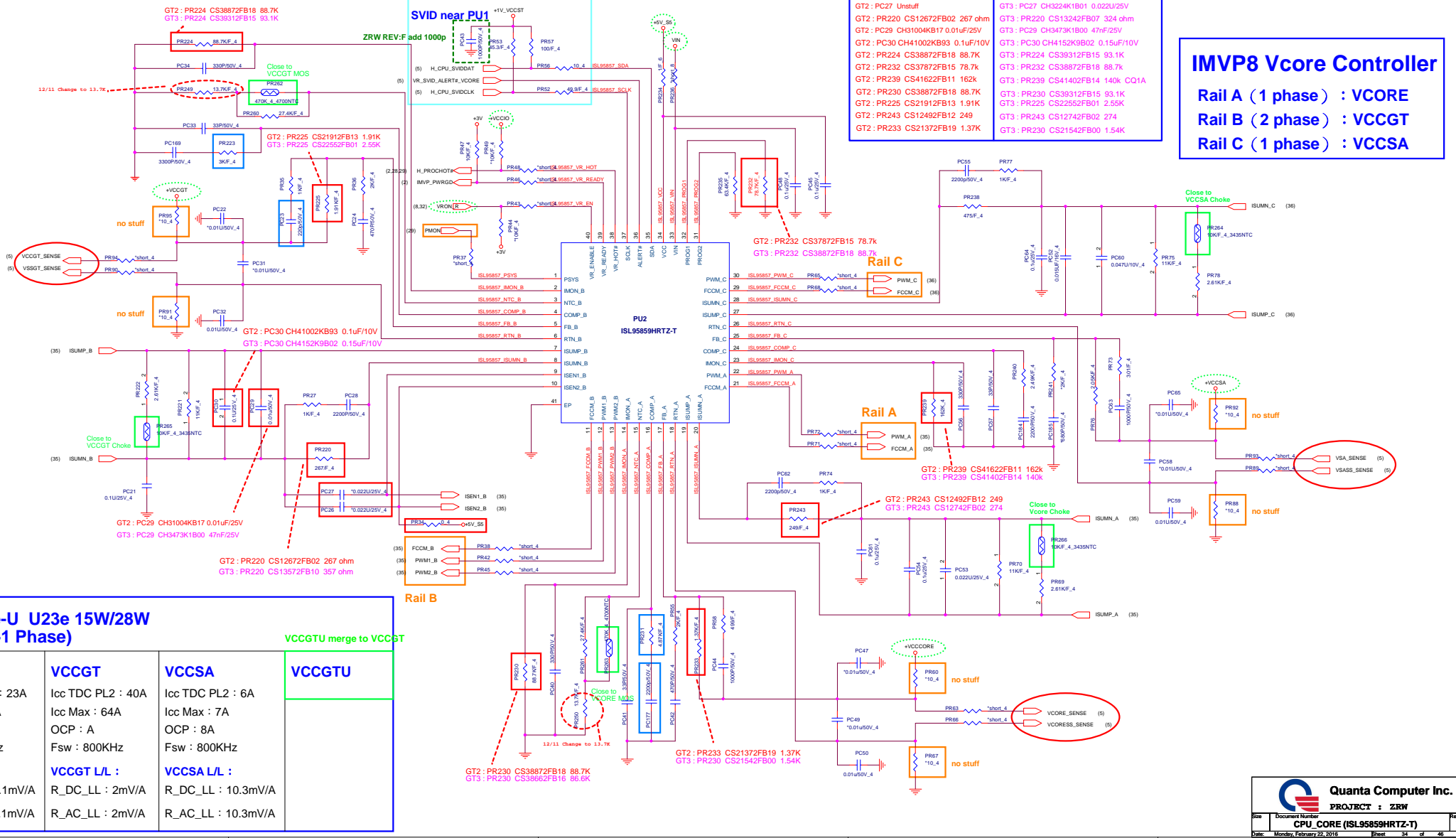
## +2.5VSUS Power Rail For DDR4



## 10/26 Reserve +2.5V for DDR4 VDDSPD

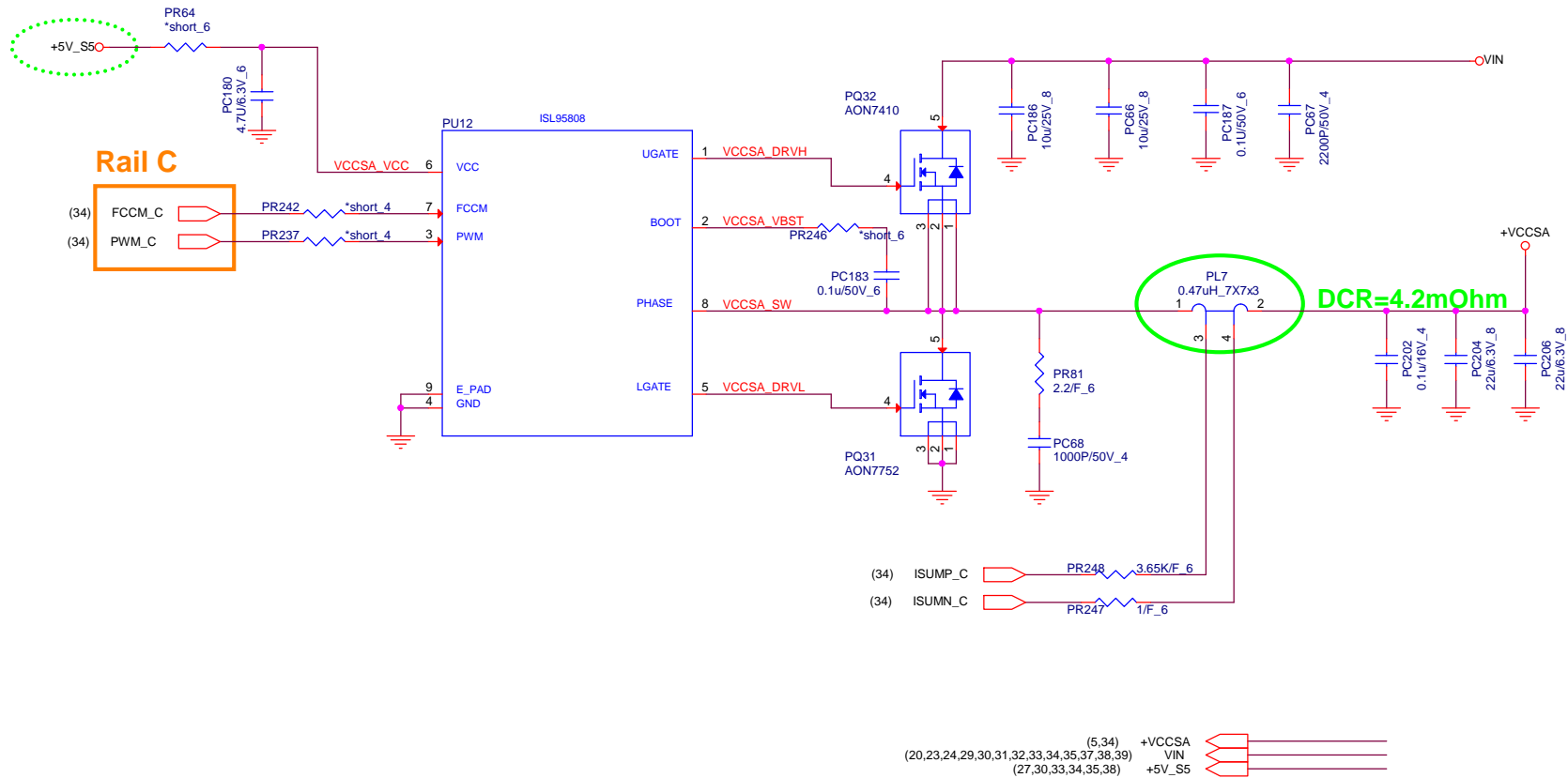


Check PU high with HW





# VCCSA



## VCCSA

Icc TDC PL2 : 5A

Icc Max : 5A

OCF : 6A

Fsw : 800KHz

VCCSA L/L :

R\_DC\_LL : 10.3mV/A

R\_AC\_LL : 10.3mV/A

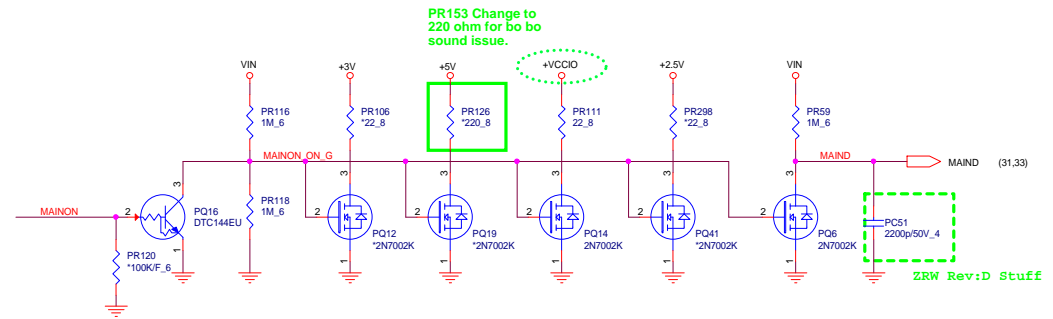
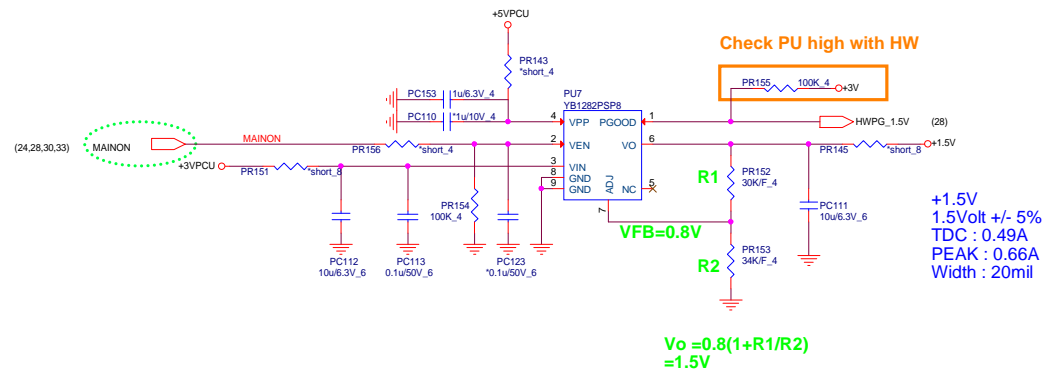


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**PROJECT : ZRW**

Size	Document Number	Rev
	<b>VCCSA (ISL95808HRZ-T)</b>	1A

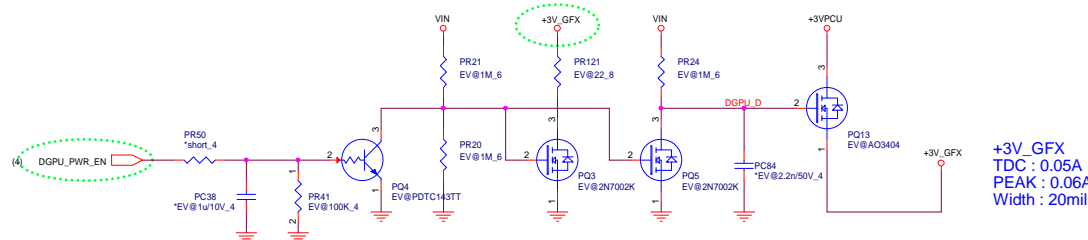
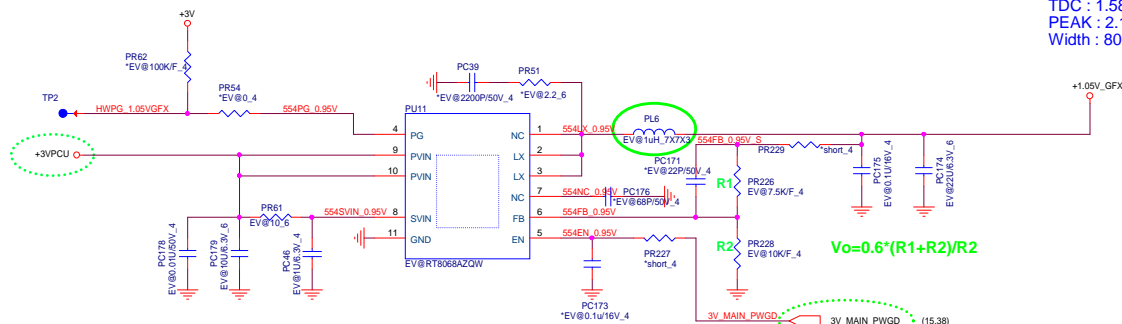
Date: Monday, February 22, 2016 Sheet 36 of 46





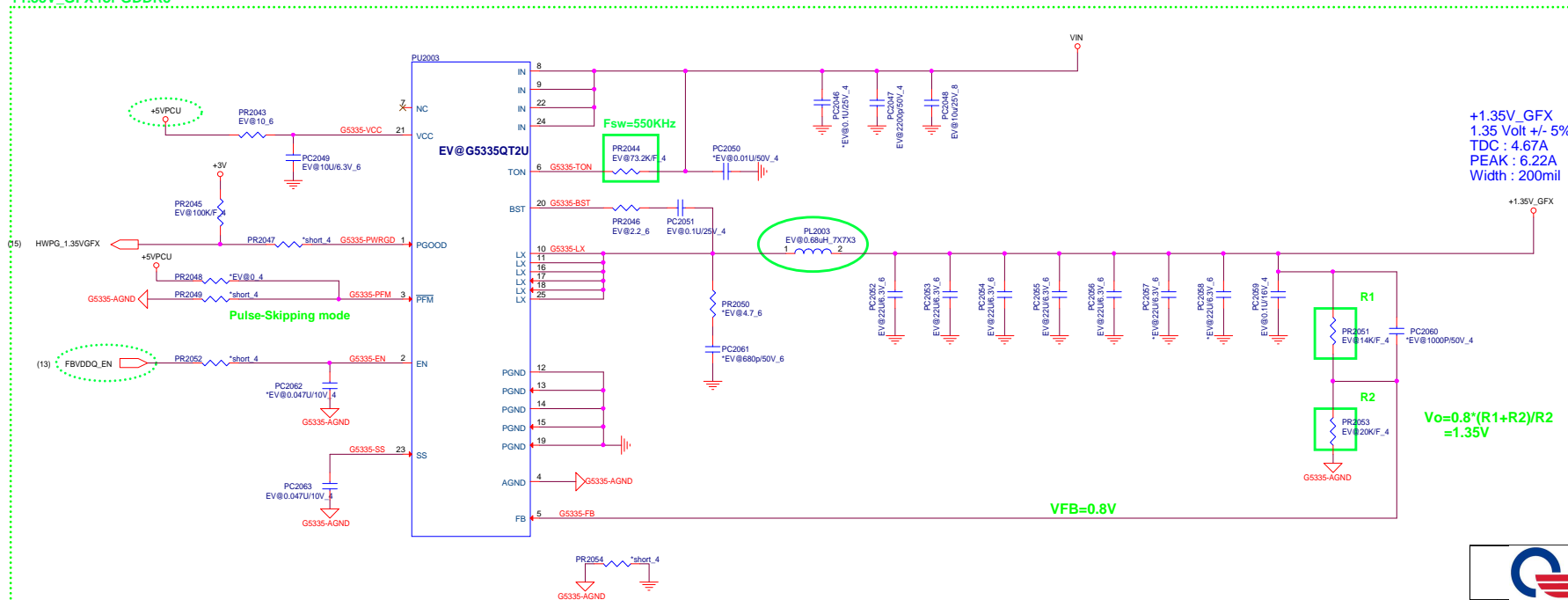
(13,14,15) +1.05V\_GFX  
(13,15,16,29) +3V\_GFX  
(14,16) +1.35V\_GFX

+1.05V\_GFX  
TDC : 1.58A  
PEAK : 2.1A  
Width : 80mil



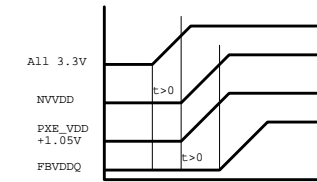
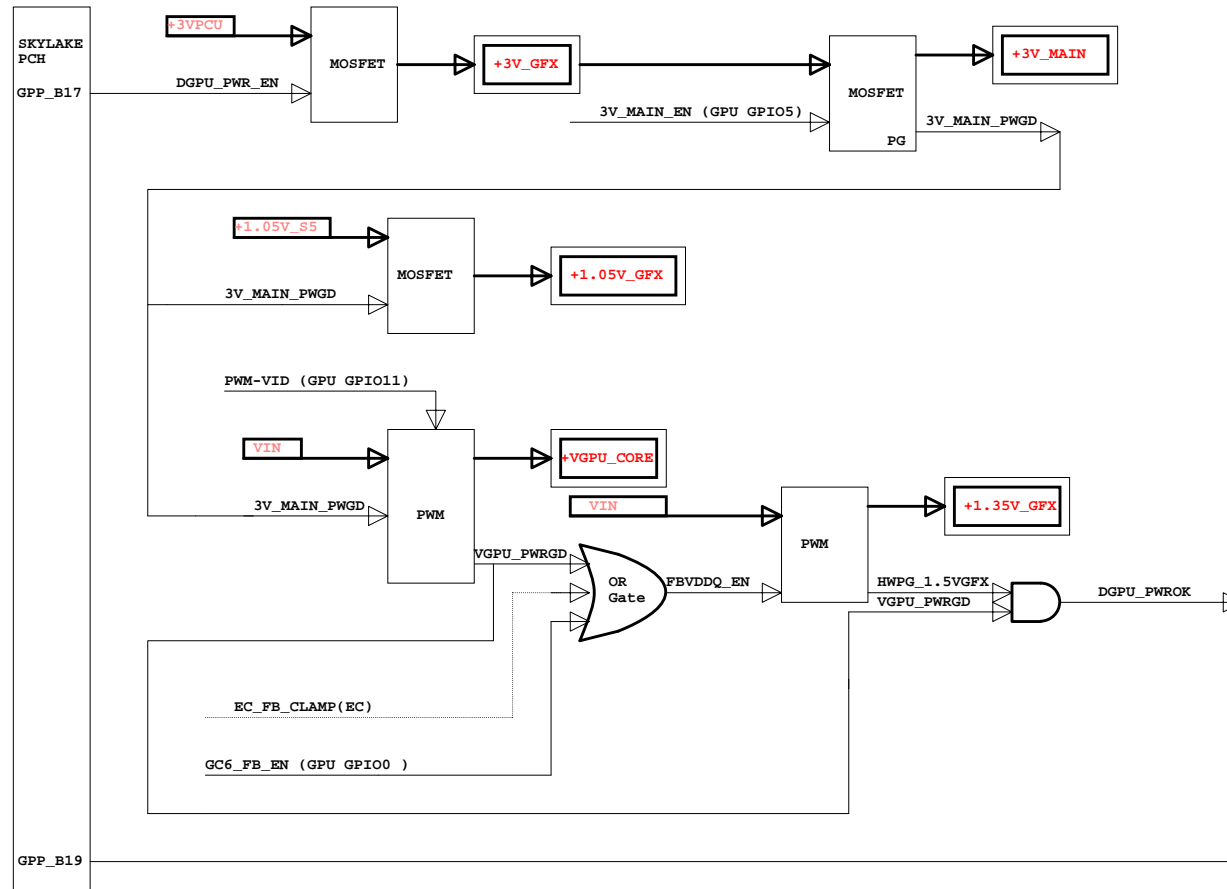
+3V\_GFX  
TDC : 0.05A  
PEAK : 0.06A  
Width : 20mil

+1.35V\_GFX for GDDR5



+1.35V\_GFX  
1.35 Volt +/- 5%  
TDC : 4.67A  
PEAK : 6.22A  
Width : 200mil

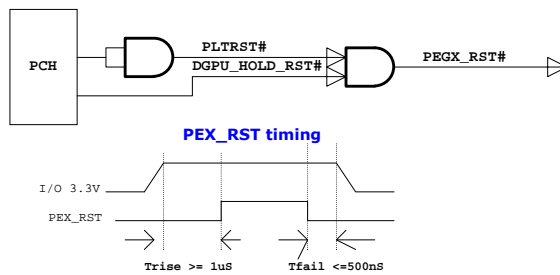
### VGA power up sequence



N15x Power on sequence

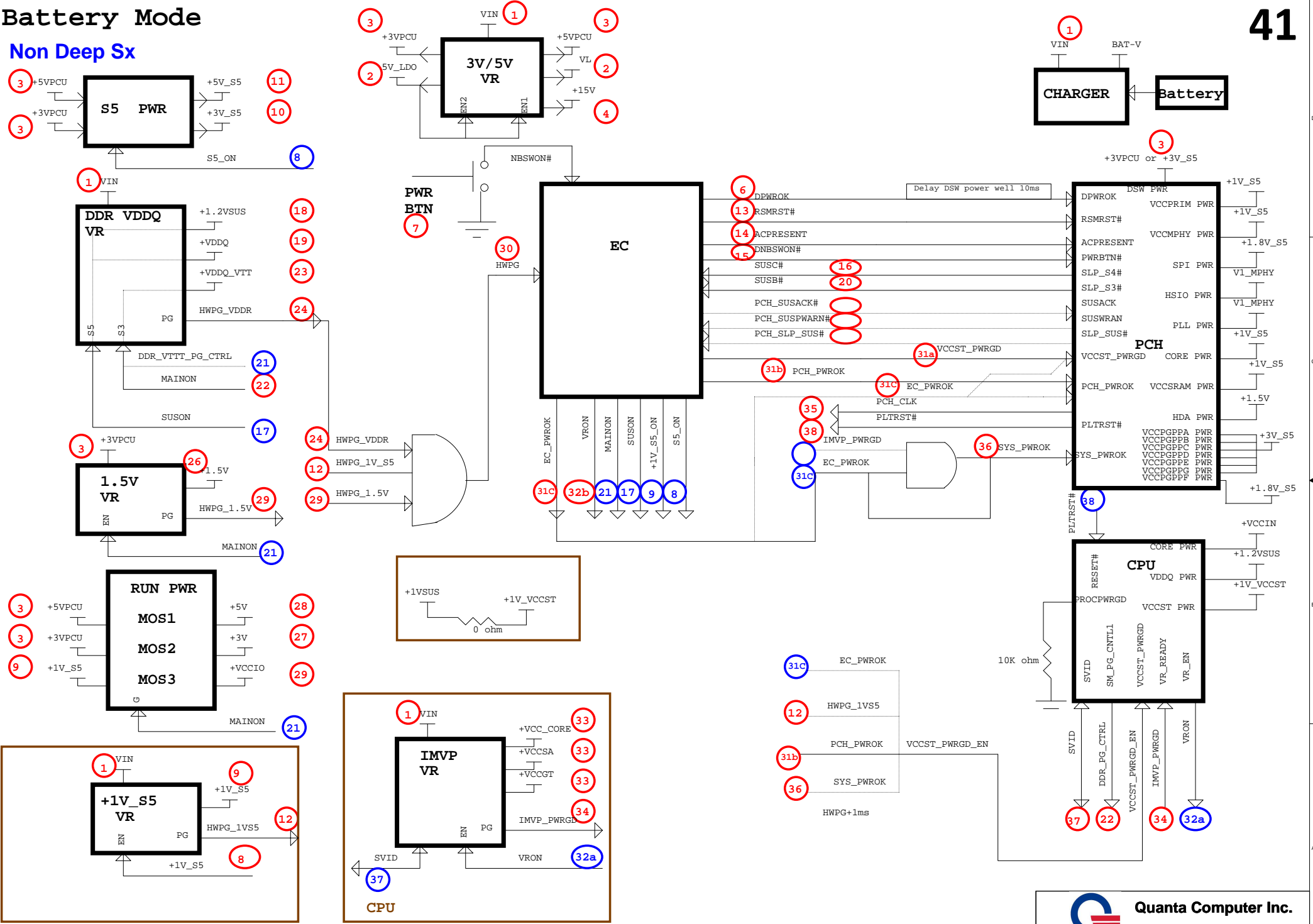
Notes: -All 3.3V includes all rails powered at 3.3V  
-PEX\_VDD 1.05V includes all rails that are shared

### VGA Reset

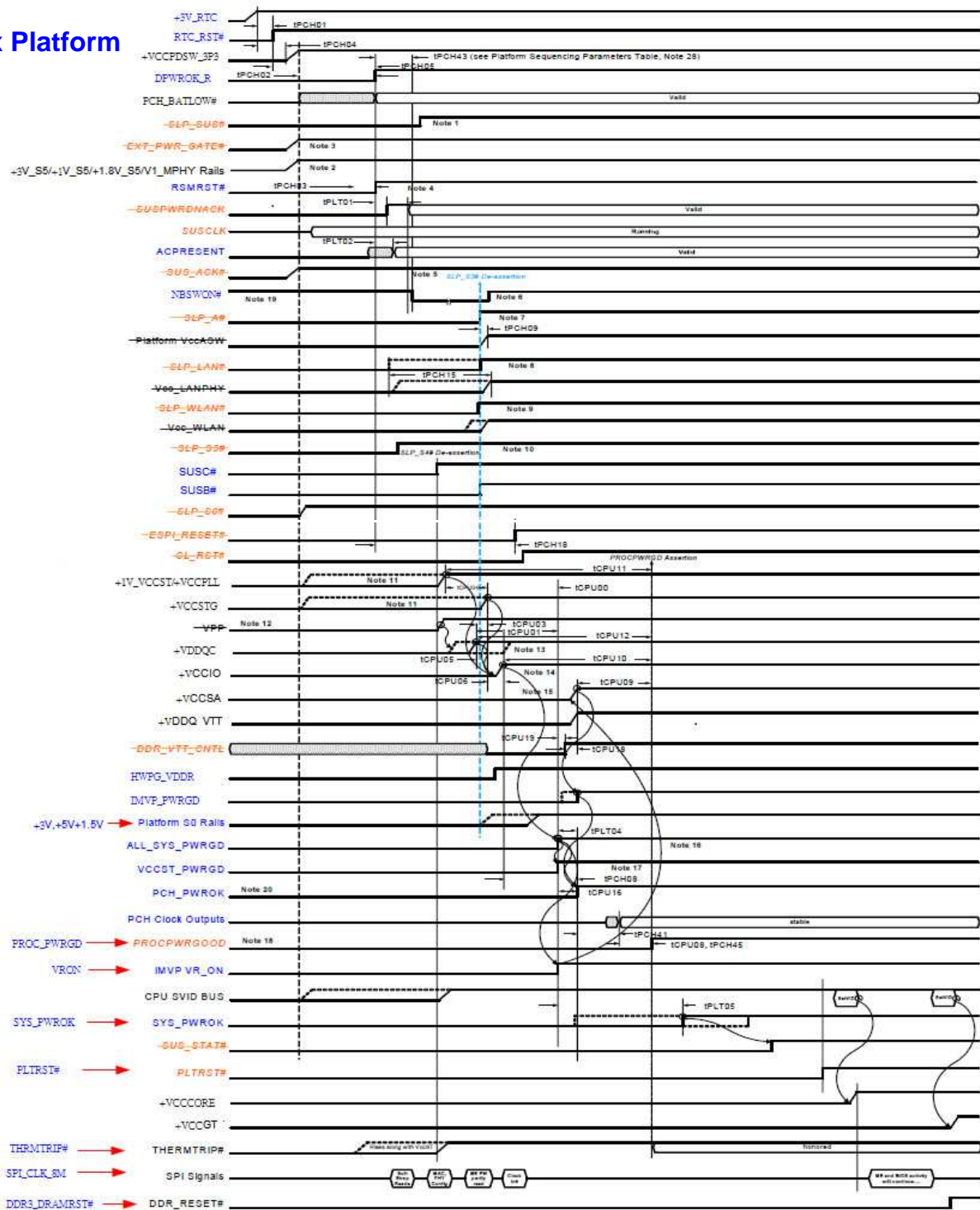


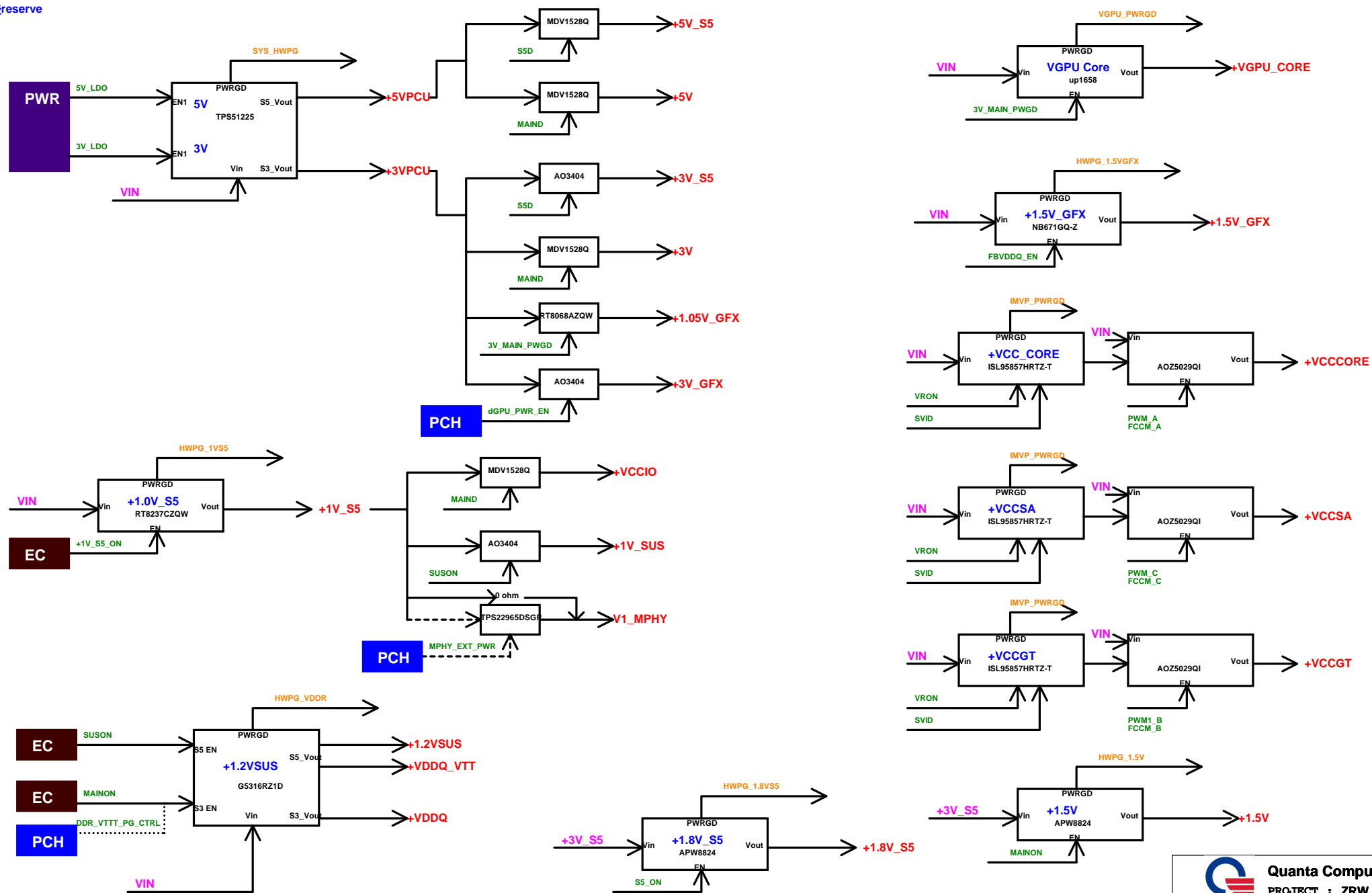
Battery Mode

Non Deep Sx

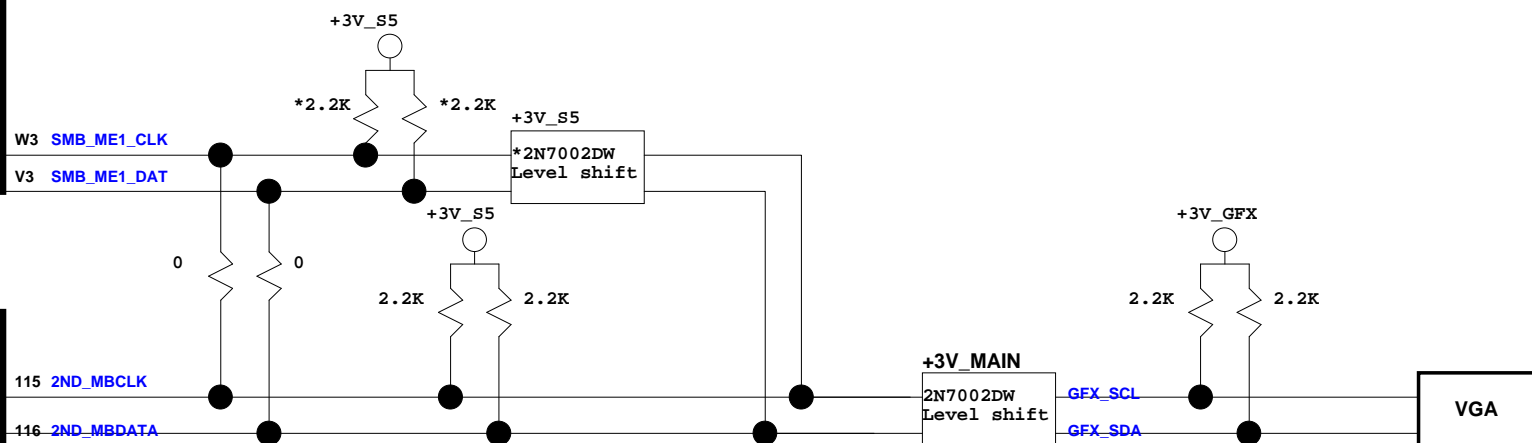
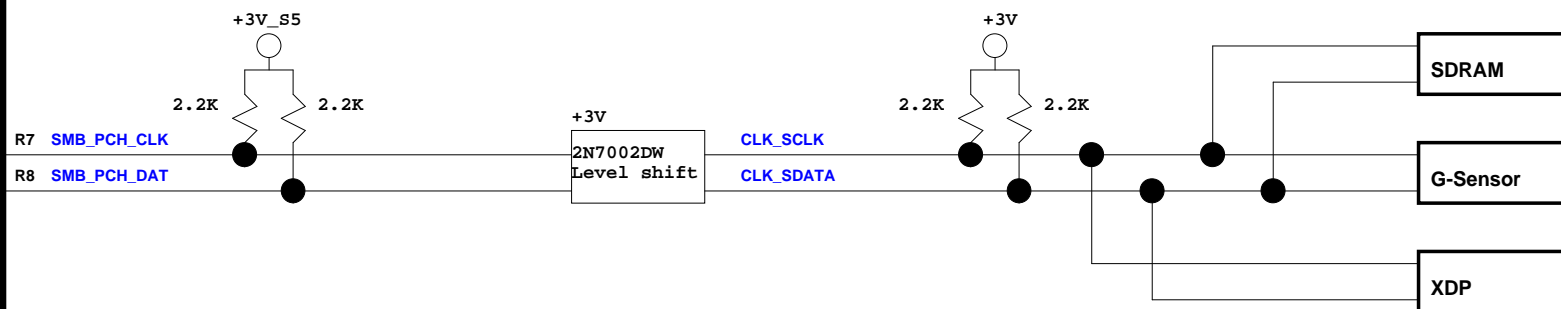


# Skylake U Non-Deep Sx Platform Power on sequence





Skylake U

EC  
IT8987CX